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Impact of silicon nitride stoichiometry on the effectiveness of AlGaN/GaN HEMT fieldplates

William M. Waller, Mark Gajda, Saurabh Pandey, Johan J. T. M. Donkers, David Calton, Jeroen Croon, Serge Karboyan, Jan Šonský, Michael J. Uren, Member IEEE, and Martin Kuball, Senior Member IEEE

Abstract—Fieldplate control of current collapse and channel electric field distribution in AlGaN/GaN HEMTs is investigated as a function of LPCVD silicon-nitride stoichiometry. Dependence of current collapse is seen, however this also leads to enhanced fieldplate pinch-off voltages and higher leakage. Electric field concentration at the gate edge is indicated by measuring off-state 2DEG position with a sense contact technique. A model explaining the fieldplate threshold variation due to barrier leakage is proposed.

Index Terms—AlGaN/GaN HEMT, field plate, passivation.

I. INTRODUCTION

There has been much interest in AlGaN/GaN based transistors for high power applications, in part due to GaN’s superior critical breakdown field of 3.3 MV/cm [1]. However strong electric fields, which exist in devices during operation can be the cause of reliability problems such as leakage, charge trapping and device degradation [2-4]. Some of these problems can be reduced by building devices with well optimized field plates (FPs) [5,6], together with a SiN₃ passivation/encapsulation deposition process. Previous work on the silicon nitride deposition process has measured DC characteristics and current collapse [7-12]. Here, in addition to this we demonstrate the impact of SiN₃ changes to the channel electric field profile which is critical to device reliability. Importantly, this work shows that modifying the silicon nitride process can change the FP pinch-off voltages.

Introduction of FPs into devices has been shown to dramatically increase breakdown voltage by spreading the region where potential is dropped away from the edge of the gate. Models usually assume a purely capacitive effect, given by electrostatics, where the difference in potential between the FP and the channel defines the depletion of electrons in the 2DEG. The drain voltage when the channel pinches off under the FP, VFP is given by

\[ V_{FP} = \frac{e n_s}{C_{FP}}, \]

where \( e \) is the electron charge density of the channel and \( C_{FP} \) is the channel to FP capacitance per unit area. \( C_{FP} \) is calculated by the in-series addition of capacitance of each layer. Capacitance of each layer is given by \( \frac{\varepsilon}{d} \) where \( d \) is the thickness of the layer and \( \varepsilon \) is the dielectric constant of the layer. In this paper, we demonstrate a fieldplate pinch off voltage different from Eq. 1 that is dependent on the stoichiometry of the silicon nitride deposited onto the AlGaN surface.

In this study, we investigate the consequence of the leaky

Fig. 1. (a) Normalized dynamic \( R_m \) of HEMTs fabricated on wafers with low leakage, A, and high leakage, D, LPCVD nitride. Stress conditions \( V_{GS} = 5 \) V, \( V_{DS} = 100 \) V for 1000s. Measurement conditions \( V_{GS} = 0 \) V, \( V_{DS} = 1 \) V. (b) Drain-gate leakage current of the same devices.

Fig. 2. Cross-section of normal HEMT device. Expansion of device regions; Schottky contact (SC), gate wing (GW), fieldplate1 (FP1) and fieldplate2 (FP2).

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William Waller, Serge Karboyan, Michael J. Uren and Martin Kuball are with the I.H. Wills Physics Laboratory, University of Bristol, Bristol BS8 1TL, U.K. (e-mail: WW0206@bristol.ac.uk;).

Mark Gajda, Saurabh Pandey, Johan J. T. M. Donkers, David Calton, Jeroen Croon and Jan Šonský are with NXP Semiconductors. This work was supported in part by the Engineering and Physical Sciences Research Council (EPSRC) and in part by NXP semiconductors.
dielectric on the effectiveness of the FPs and show that the voltages at which they become effective are strongly influenced by passivation nitride stoichiometry with consequences for device reliability. Effectiveness in this context is the ability of the FP to reduce the lateral electric field at edge of the gate metal, increased FP threshold voltages seen here lead to a doubling of this electric field. This effect is linked to changes in current collapse and leakage through the device.

II. GROWTH AND FABRICATION

Measurements were made on 4 wafers which were grown with identical epitaxy. These were 150nm diameter GaN-on-Si wafers grown by metal organic chemical vapor deposition with a strain relief layer, a carbon doped buffer and uid-GaN layer, followed by a 20 nm AlGaN layer and a 3 nm GaN cap, giving a total epitaxial thickness of ∼5µm; 2DEG carrier density was 5.87 × 10^{12} cm^{-2}. Subsequently a 70 nm low-pressure chemical vapor deposition (LPCVD) silicon nitride was deposited using a horizontal LPCVD furnace at 850°C, with an approximate pressure of 100mTorr. The wafers were soaked in NH₃ before introduction of the dichlorosilane (DCS). The stoichiometry of this silicon nitride was varied between the wafers and was the only difference between the wafers. The stoichiometry was controlled by varying the DCS/NH₃ precursor ratio while keeping a constant gas flow rate. Wafer A received the stoichiometric Si₃N₄ ratio and the DCS fraction was increased systematically up to wafer D with the highest Si content, given in Table 1. Devices and test structures were fabricated using a metal, increased FP threshold voltages seen here lead to a doubling of this electric field. This effect is linked to changes in current collapse and leakage through the device.

III. EXPERIMENTS AND RESULTS

Dynamic resistance measurements were made on HEMTs after a stress condition of VGSS=−5V, VDS= 100V had been applied for 1000s, these are shown in Fig. 1(a). A trade-off between leakage and current collapse is seen as DCS/NH₃ ratio is varied. The high current collapse in wafer A is reduced in D by increasing the DCS/NH₃ ratio, however this is also seen to increase the off-state drain current seen in Fig. 1(b). Details of the exact mechanism will be investigated in future work.

Capacitance was measured in large anode-width Schottky diodes (30mm) and is shown in Fig. 3. These had two anode FPs which extended along the channel, the first (FP1) was deposited after a PECVD Si₃N₄ of 300 nm, the second (FP2) was after another 300nm of Si₃N₄, giving a total thickness of Table 1:

<table>
<thead>
<tr>
<th>Wafer</th>
<th>DCS/NH₃</th>
<th>Stress (MPa)</th>
<th>Refractive Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.33</td>
<td>1132</td>
<td>2.01</td>
</tr>
<tr>
<td>B</td>
<td>2.49</td>
<td>428</td>
<td>2.10</td>
</tr>
<tr>
<td>C</td>
<td>3.30</td>
<td>275</td>
<td>2.14</td>
</tr>
<tr>
<td>D</td>
<td>4.38</td>
<td>117</td>
<td>2.21</td>
</tr>
</tbody>
</table>
693nm from FP2 to the 2DEG. FP geometry is that of the HEMT in Fig. 2 but here the gate and fieldplates are in electrical contact, which allows easy capacitance measurements in a structure that is electrically very similar to the HEMT in off state operation. Also plotted is the theoretical capacitance in the case of zero leakage or charge trapping based on Eq. 1 using the dimensions of the field plates. The value of each theoretical capacitance step fits the measured values well, however there is strong positive and negative deviation in the FP pinch-off voltages in each of the devices from this theoretical curve. Wafers C&D show a large increase in the threshold voltage of FP1 and FP2 indicating a temporary positive charge storage, whereas wafers A, B show a small negative shift.

Measurements of 100µm×100µm fatFET devices with gate stacks equivalent to the HEMT gate wing, FP1 and FP2 are shown in figures 4, 5 & 6 respectively. The negative threshold voltage of these transistors corresponds to the required positive voltage applied to the drain in a HEMT to induce retraction of the 2DEG from under that FP. For the gate wing devices there is no significant threshold change, any change can be explained by manufacturing differences in the thickness, displayed in the inset. A lack of threshold hysteresis or shift here strongly indicates no charge trapping at the AlGaN /LPCVD SiN₃ interface and that any interface charge here was kept constant between the wafers. In the case of the FP devices there are both positive and negative shifts in the expected threshold voltages with respect to a purely capacitive model, suggesting multiple mechanisms altering the threshold voltage. Wafers A&B have a threshold close to the purely capacitive case, and show hysteresis indicating negative charge storage, with the possible exception of wafer B FP1. Whereas wafers C&D (with high DCS/NH₃ ratio) have a much larger threshold voltage, and show a small hysteresis, indicating positive charge storage. The smaller hysteresis in wafer B FP1 may indicate the trapping process is field dependent and has more contributions than just at the surface.

In order to monitor this retraction of the 2DEG in a working device, special Schottky gate HEMTs were fabricated. These are HEMTs with an extra Schottky sense-contact positioned under FP2, shown inset in Fig. 7. This device design has been used in a previous study [15]. Here, this extra contact is biased in current mode such that a small current (10⁻⁷A in this case) flows from the channel across the forward biased Schottky barrier. The potential measured, \( V_{\text{sense}} \), is then within 1V of the channel potential under this sense-contact. The gate is biased at -7V to pinch off the channel, source is at 0V and the drain voltage is swept to 400V, with \( V_{\text{sense}} \) shown in Fig. 7. Before the 2DEG has retracted past the sense finger the potential measured at that contact should be almost equal to the drain potential (i.e. \( V_{\text{sense}} = V_D \)). At the point where the 2DEG retracts past this sense contact the potential will show a reduction in gradient. This knee indicates that the channel potential at the sense contact is no longer in good electrical connection to the drain, thus the potential \( V_{\text{sense}} \) rises more slowly than the drain potential. It can be seen clearly from Fig. 7 that the wafers with low DCS/NH₃ ratio, A&B, have a sharp knee at around 60V, whereas high DCS/NH₃ wafers, C&D, have a less well defined knee indicating slower 2DEG retraction and a resultant stronger electric field at the gate edge, broadly consistent with the data of Fig. 6.

The Schottky leakages are displayed in Fig. 8. These were measured on 100µm×100µm fatFET devices. There is clear ranking in Schottky reverse bias leakage between the wafers, with leakage increasing from A to D. As the LPCVD SiN₃ was the only step which varied between these wafers the difference in its leakage was measured. Due to the processing sequence this leakage was measured in series with the AlGaN barrier and the results are shown in Fig. 9. This MIS junction was forward biased to reduce the contribution to resistance from the AlGaN barrier. The AlGaN barrier has a much lower resistance than the SiN₃, for example by comparing Figs 8 and 9 at a current of 1Acm⁻² less than 1V is dropped across the AlGaN. The highest DCS/NH₃ ratio wafer D has ~six orders of magnitude more LPCVD SiN₃ leakage current than the lowest ratio, A. There is significant leakage through this...
layer for wafers C and D at the point the channel would retract (~11.5V), contributing to the higher off-state leakage seen in Fig. 1(b).

The leakage through the 300nm PECVD layer present in FP1 was measured on a metal-insulator-metal structure and is presented in Fig. 10. The resistance is higher than for the LPCVD layer due to increased thickness. The minor variation seen here is due to small manufacturing differences. This layer is shown to be very resistive until a voltage of 60V or more is dropped across it.

IV. DISCUSSION

The key observation is that FP threshold voltages for the highest DCS/NH3 ratio wafers, C&D, shift to higher voltages with respect to the purely capacitive value implying temporary positive charge storage. This shift can be seen in capacitance and fastFET measurements in Figures 3, 5 and 6 but is not seen in the gate wing devices plotted in Fig.4. We note that the different SiNx layers between the FP and the 2DEG will have different conductivity, so when biased, charge can accumulate within the dielectric stack and this can cause an increase in $V_{FP}$. A circuit model is shown in Fig. 11(c). When the charge stored across the combined capacitor of the AlGaN and LPCVD SiNx layers, $C_{GW} V_{GW}$, is equal to the initial channel electron density, $n_e$, the 2DEG is depleted and will retract from under the FP towards the drain. For a leaky device dielectric this new threshold voltage is calculated by considering the potential across the lower part of the stack, $V_{GW}$, when the conducting stack acts as a potential divider.

$$V_{GW} = \frac{R_{GW}}{R_{PECVD} + R_{GW}} V_D$$

(2)

This leads to a modified expression of Eq. 1 valid in the steady state:

$$V_{FP} = \left(1 + \frac{R_{PECVD}}{R_{GW}}\right) \frac{e n_e}{C_{GW}}.$$  

(3)

where

$$R_{GW} = R_{AlGaN} + R_{LPCVD} \text{ and } C_{GW} = C_{AlGaN} C_{LPCVD} \left(\frac{1}{C_{AlGaN}} + \frac{1}{C_{LPCVD}}\right).$$

$R_{label}$ and $C_{label}$ are the resistances and capacitances of each of the layers labelled in Fig. 11(b). Eq. 3 applies when the RC time constant of each of the layers is shorter than the time held at each measurement voltage. Whereas Eq. 1 applies instantaneously after switching. An increase in the leakage through the AlGaN and LPCVD SiNx barriers results in $R_{PECVD} \gg R_{GW}$ and so, from Eq. 3, $V_{th}$ increases. Each of the layer resistances are field dependent and lead to field-dependent time constants that have been plotted in Fig. 12, calculated from measured resistances and known thicknesses of the layers. The FP stack will either be described (i) by Eq. 1 if each layer is highly resistive, (ii) by Eq. 3 if it has reached a steady state or (iii) it will be in a transient state where the charges and fields in the stack are changing. The RC time constants marked by diamonds in Fig. 12 for each LPCVD SiNx layer indicate the response-time at the electric field required to pinch-off the channel, this is very high for wafers A and B, on the order of a minute and above, explaining why Eq. 3 applies to wafers C and D only.

Fig. 11(a) is a plot of Eq. 3 as the ratio of resistances in the dielectric stack, $\frac{R_{PECVD}}{R_{GW}}$, is varied. This agrees reasonably well with the measured $V_{th}$ values for wafers C and D. For the highest DCS/NH3 ratio wafers the lower part of the barrier is leaky (AlGaN and LPCVD SiNx) and the potential is mainly dropped over the PECVD nitride layer, away from the channel, resulting in positive charge accumulating at the PECVD/LPCVD SiNx interface and thus requiring a much larger voltage to deplete the channel. Whereas for low DCS/NH3 ratio wafers A&B the AlGaN barrier and LPCVD nitride are more resistive and the stack responds closer to the purely capacitive model. It can be seen from Fig. 9 that wafers A and B do not have significant leakage across the nitride before the channel in a device is pinched-off, at a potential difference of ~ 11.5 V, once pinched-off any increase in drain potential is dropped elsewhere in the device. Fig. 12 also indicates that the time constants for charge to accumulate across the LPCVD SiNx layer are very long for these wafers at pinch-off. These observations explain the absence of increased FP threshold in wafers A and B; without leakage across this LPCVD SiNx layer positive charge cannot be stored at the LPCVD/PECVD SiNx interface.

This difference in conductivity through the different layers provides an explanation for the hysteresis observed in Figs 3, 5.
and 6 i.e. transport to traps rather than the trapping kinetics is the rate-limiting step, in contrast to systems where the de-trapping process is dominant [16]. This model is supported by the lack of shift in the gate wing threshold in Fig. 4. The positive charge is presumably caused by electrons vacuuming traps at the SiN/SiN interface. For high DCS/NH2 ratio wafers, C&D, any positive charge stored at the LPCVD/PECVD SiN interface leaves the structure quickly after a sweep due to the high leakage of the lower part of the stack even at relatively low fields meaning small positive-charge hysteresis. Conversely, when the AlGaN and LPCVD SiN are more resistive than the PECVD SiN, a layer negative charge can become trapped at the LPCVD/PECVD SiN interface due to leakage in the PECVD SiN, under high electric fields, this charge cannot quickly escape the structure as the time constants when in this state are much longer, layers only conduct under high electric field via a Poole-Frenkel mechanism. The negative-charge hysteresis and Vth shift seen in Figures 3, 5 and 6 can be explained by this mechanism. In this paper we have considered charge storage above the channel, charge storage in the GaN:C buffer can cause a dynamic on-resistance [17].

Methods for controlling current collapse and leakage in AlGaN/GaN HEMTs include gate edge shaping [18], optimization of the buffer [19], and optimizing epitaxial thickness [20]. Modifying the stoichiometry of the LPCVD SiN provides an additional parameter which should be considered when optimizing devices for current collapse and leakage. However, this SiN can change the off-state lateral and vertical electric field profile due to enhancement of FP pinch-off voltages, this effect should be considered when maximizing reliability with FP structures.

V. CONCLUSION

The LPCVD silicon nitride’s DCS/NH2 ratio has a strong effect on fieldplate pinch-off and has an influence on the current-collapse and leakage tradeoff in GaN HEMTs. Changing the nitride stoichiometry changes the dielectric leakage, and in a multilayer dielectric stack this will modify the FP threshold voltages, introduce an unwanted time dependence and alter electric field control in the channel, modifying FP optimization.

**William M. Waller** received the M.Sc degree in Physics from the University of Bristol, Bristol, U.K., in 2014. He is currently working toward the Ph.D. degree in physics at the Centre for Device Thermography and Reliability.

His research interests currently focus upon characterization and reliability of AlGaN/GaN HEMTs and MISHEMTs.

**Serge Karboyan** received the M.Sc. and Ph.D. degrees in physics from the University of Toulouse, Toulouse, France. He was formerly with LAAS-CNRS in France, where he worked on GaN based devices. He is currently a Research Assistant with the University of Bristol, Bristol, U.K.

**Michael J. Uren** (M’06) received the M.A. and Ph.D. degrees in physics from the University of Cambridge, Cambridge, U.K. He was formerly with RSRE, DERA, and QinetiQ, where he worked on Si, SiC and GaN devices. He is currently a Research Professor with the University of Bristol, Bristol, U.K. He is a Fellow of the Institute of Physics.

**Martin Kuball** received the Ph.D. degree from the Max-Planck Institute in Stuttgart, Germany. He is Professor in Physics and the Director of the Center for Device Thermography and Reliability at the University of Bristol, Bristol, U.K. He holds the Royal Society Wolfson Research Merit Award.