A 2GHz GaN Class-J Power Amplifier for Base Station Applications
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1. INTRODUCTION

Need for reduction of base station power consumption while increasing QoS
- Power Amplifier is a major power consumer
- High order constellations are necessary
- Channel bandwidths keep increasing

Efficient
  Linear
  Wideband

2. CLASS-J THEORY

Class-J
- Recently introduced (2006)
- Complex fundamental impedance
- Reactive 2nd harmonic
- Continuous “design space”
- Multiple impedance pairs ($Z_{fo}$, $Z_{2fo}$)
- Class-B-like output power and efficiency
- Class-B / J / J* are specific sub-cases

$Z_{fo} = 0.9142 + 45^\circ$
$Z_{2fo} = 1.1781 - 90^\circ$

3. METHODOLOGY – REALIZATION OF THE POWER AMPLIFIER

- Large signal transistor model
- Extrinsic parasitics and package model
- Intrinsic drain impedances given from theory
- No active harmonic load-pull
- No RF waveform probing
1. Deep Class - AB biasing
2. Determine appropriate load-line
3. Intrinsic drain impedances based on theory
4. 3rd output harmonic impedance
5. Source-pull for efficiency/gain
6. Observe intrinsic drain waveforms
7. Design matching networks

- 3rd harmonic not defined by theory
- 3rd harmonic reflection coefficient angle swept
- Affects efficiency / output power
- Chose an insensitive/efficient case

- Intrinsic drain waveforms
- De-embedded in simulations to prove Class of operation
- No “zero” voltage crossing
- Similar to expected waveforms
- Some 3rd harmonic present
- Current “hump”

- Distributed matching networks
- 2 harmonics controlled at the input, 3 at the output
- RT/Duroid 8550 substrate
- $E_r = 2.2$, $T = 787\,\text{mm}$
- Size : $13.5 \times 6.5\,\text{cm}$
- Higher $E_r$ will reduce size

4. PERFORMANCE

- 65% maximum PAE
- 40dBm output power
- Good back-off performance
- Low asymmetry up to 20MHz
- Low memory effects
- Facilitates linearization
- 60%+ efficiency over 140MHz
- 39-40dBm output power over band
- LTE and LTE-Advanced

5. CONCLUSIONS

- More freedom in PA design / No need for specific impedances
- Theory and extrinsic parasitic model is sufficient
- 3rd output harmonic impedance is important

- 65% PAE, over 70% drain efficiency, 40dBm output power
- Low memory effects
- Promising under ET/EER implementations