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Investigating GaN power device double-pulse testing efficacy in the face of V_{TH}-shift, dynamic R_{dson}, and temperature variations

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***Abstract*— Double-pulse testing is widely used in the power-electronics industry for rapid evaluation of power devices. These tests aim to allow observation of how a power device under test (DUT) would behave in real-world continuous-mode operation, without having to operate a full converter. It is well known that several device parameters are temperature-dependent, and for full accuracy, in the double-pulse test the temperature of the DUT must be controlled such that it matches the temperature(s) expected in real-world operation. Further and more challenging complications arise if a GaN (Gallium nitride) transistor is being tested, as these suffer from electron/hole trapping between different layers of the device (e.g., p-GaN, GaN, AlGaN), which can modulate the gate voltage threshold (V_{TH}) up or down, and give rise to the phenomenon known as dynamic R_{dson}. This paper reviews the factors that give rise to these dynamic effects in the two main families of normally-off p-gate GaN power transistors: Schottky-gate and ohmic-gate. Experiments performed with a 400 V, 2 kW-rated converter, whose power devices are mounted on a daughter-board so they can be interchanged without affecting the power board, demonstrate the types and levels of discrepancy to be expected between double-pulse testing and continuous-mode operation. Modification of the double-pulse test to an N-pulse test is proposed, and it is shown that this new test method can reproduce the waveforms seen during continuous operation.**

Keywords—wide band gap, GaN, gate threshold shift, di/dt infinity sensor.

I. Introduction

New high-performance materials for power transistors, such as silicon carbide (SiC) and gallium nitride (GaN) [1], [2], have permitted a step-increase the efficiency and power density of power conversion. Enhancement-mode GaN HEMTs are made by growing a p-type GaN (p-GaN) gate on an AlGaN barrier, raising the gate threshold voltage (V_{TH}) from sub-zero to above zero. These devices, compared to cascode devices [3], have lower package inductances, lower device capacitances, lower V_{TH}, and lower gate voltage requirement. However, p-GaN gate devices experience V_{TH} instability [4]–[6] and dynamic R_{dson} [7], [8], due to electron/hole injection and depletion at different layers of the devices. Throughout this paper, V_{TH}-shift and dynamic R_{dson} are referred to collectively as “dynamic effects”. These dynamic effects result in device-history dependent behaviour, which presents a problem for the commonly-used double-pulse test.

Double-pulse tests are often used to evaluate power devices, as they employ a simple test setup, and only require a low-current power supply, since the load current of a double-pulse test being supplied by local DC-link capacitors. The purpose of the test is to enable observation of how a power device under test (DUT) will behave in real-world continuous-mode operation, without having to embed the device in a full power converter. As several device parameters are temperature dependent [9], for maximum accuracy it is important to ensure that the DUT temperature matches that expected during continuous-mode operation. However, if the DUT is a p-gate GaN device, even with temperature matching the waveforms observed in a double-pulse test may not match those seen in continuous-mode operation because the device histories do not match so the device threshold and other parameters can be significantly different in the two operating scenarios.

The contributions of this paper are:

- In Section II, a review of dynamic effects in p-gate GaN devices, together with an experimental demonstration of V_{TH}-shift effects in a Schottky-gate device (a GaN Systems 650 V, 50 mΩ GS66508T [10]), and in an ohmic-gate device (an Infineon 600 V, 70 mΩ IGOT60R070D1 [11]).
- In Section III, presentation of a test board concept that mounts the power devices under test on a daughter board, allowing for easy interchange of the DUT, and minimisation of the number of variables involved when comparing device behaviours. The board is rated at 2 kW and is carefully designed to deliver fast, clean switching despite the daughter-board arrangement. Using SiC MOSFETs as a control, it is shown that when the power devices under test do not exhibit dynamic effects, the measured waveforms for continuous-mode operation and double-pulse tests are identical.
- In Section IV, presentation of measured results showing that, under a variety of different conditions, there can be discrepancy between continuous-mode operation and double-pulse tests for both types of normally-off GaN devices.
- In Section V, presentation of measured results showing conditions under which pulse testing delivers a closer match to continuous-mode operation. This includes a new pulse testing method that improves the match whilst retaining the benefits of double-pulse testing.

II. Overview of Dynamic Effects in p-gate GaN Power Transistors

A. V_{TH}-shift

In [4], Schottky and ohmic gate contact devices are fabricated, and it is shown that pre-biasing the gate, with a constant voltage relative to the source, results in a shift of V_{TH}. The ohmic device always shows a negative shift irrespective of the biasing voltage and duration, whereas the shift in the

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Schottky-gate device can be in either a positive or a negative direction, depending on the bias voltage and duration.

In [5], a technique is presented, to evaluate the transient threshold voltage, and three phenomena: electron trapping, hole accumulation, and hole depletion. In [6], the impact of V_{TH} modulation, due to high-voltage blocking V_{DS}, on static and switching performance of a p-GaN device, is studied. It is shown that if the gate drive voltage is higher than 5 V, then the effect of V_{DS} on the V_{TH} shift can be neglected. When a V_{DS} bias voltage is applied, the V_{TH} starts to shift, and when the bias is removed, the V_{TH} begins to revert to the initial state, but this reversion to the initial state is significantly slower than the shift induced by the biasing event [12], [13].

We would therefore expect a GaN-based power converter at start-up to have one form of switching transients, which would then settle into a different form after a period of continuous operation.

B. *Curvetracing to show V_{TH}-shift due to gate biasing*

The aim of these tests is to show the effects of gate pre-biasing on V_{TH}, using a low voltage Agilent B2902A source meter. In a first test, see Fig. 1, the gate of a Schottky-gate device is pre-biased with a pulse-train of 1.25 µs pulses (400 kHz, 50% duty). During the gate biasing, the drain and source are shorted. Immediately at the end of this biasing condition, the I_D-V_G input characteristic is measured, and V_{TH} determined, defined here as the gate voltage at a drain current of 10 mA. A family of threshold voltages is created, by sweeping the number of biasing pulses from one to 50 million, and their amplitude from 5 V to 6 V in steps of 0.2 V.

It can be observed that V_{TH} shifts up as the biasing voltage increases. Additionally, V_{TH} increases with the number of pulses. One would anticipate that the consequence of these results for a double-pulse test vs. continuous-mode operation would be as follows: a double-pulse test has an initial pulse of some 10s of µs to ramp up the current, and hence it is expected that the V_{TH} operating point for a double-pulse test will be towards the left-hand side of Fig. 1. By contrast, in steady continuous operation, the gate has been subjected to millions of gate pulses, resulting in a V_{TH} value from the right-hand side of Fig. 1.

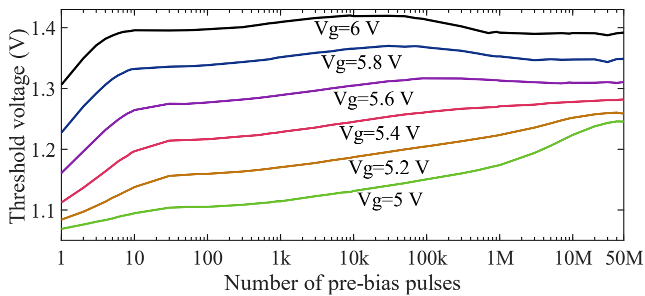


Fig. 1 V_{TH} shifts in a Schottky-gate GaN device due to pre-biasing the gate with pulse train of different magnitude and number of pulses.

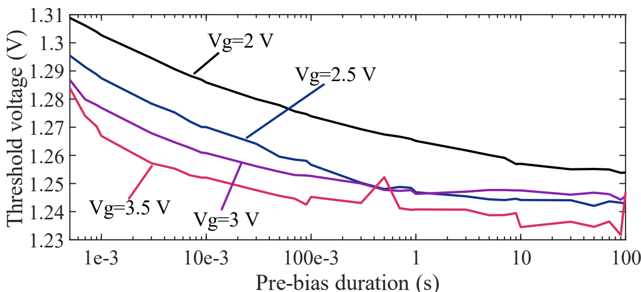


Fig. 2 V_{TH} shifts in an ohmic-gate GaN device due to pre-biasing the gate with DC voltage of different magnitude and different duration.

In a second test, see Fig. 2, an ohmic gate device is pre-biased by a single voltage pulse, after which the input characteristic and V_{TH} value are determined. This bias pulse is swept in magnitude from 2 V to 3.5 V in steps of 0.5 V, and in duration from 500 µs to 100 s. The pre-biasing is seen to shift V_{TH} downwards, the shift growing with increasing bias amplitude and duration. DC biasing was used here, as opposed to a pulse train, due to the current-driven nature of these ohmic gate devices and the limitation in the switching current output capability of the B2902A source meter.

C. *Current collapse effect on R_{DSON}*

When a GaN device is subjected to a drain to source voltage bias, electrons can trap between different layers of the device [8]. This affects the R_{DSon} and impairs the switching characteristics [6]. In normal operation of a power converter, as the devices are repeatedly subjected to a drain to source voltage, it is expected that the dynamic effects of the devices change. These must be taken into account when double-pulse testing is used to replicate the continuous-mode switching performance.

III. Hardware and Test Procedure for Comparing Double-Pulse and Continuous-Mode Switching

A. *Test-board design*

In order to test different devices in a power converter with the same PCB layout, a motherboard is designed that can carry different daughter boards, one for each type of power device under test. Together, the motherboard and a daughterboard implement a totem-pole switching cell, as shown in Fig. 3. The board can operate in double-pulse mode, or in continuous-mode operation at 2 kW. The motherboard, Fig. 4, hosts the DC link bulk capacitors, gate drivers, and the connectors for the bench power supply, load inductor, and measurement voltage probe. Connections between the motherboard and a daughter board are made using spring-loaded connectors for signal connections and soldered for power connections. The gate voltages required for each power device are different, and are adjusted using potentiometers provided on the topside of the motherboard. An Infinity Sensor [9], [14], provided on the daughter board, is used to measure the drain to source current of the low-side devices.

The following devices are tested:

1. The Schottky-gate GS66508T from GaN Systems [10].
2. The ohmic-gate IGOT60R070D1 from Infineon [11].
3. The SiC MOSFET C3M0065090J from Wolfspeed [15].

The SiC MOSFETs are used as a control, as these devices are not known to exhibit dynamic effects.

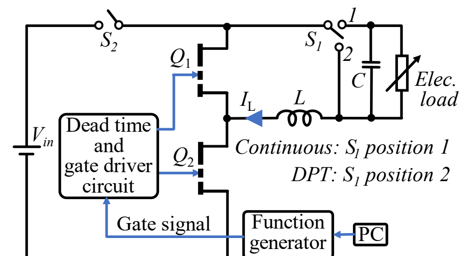
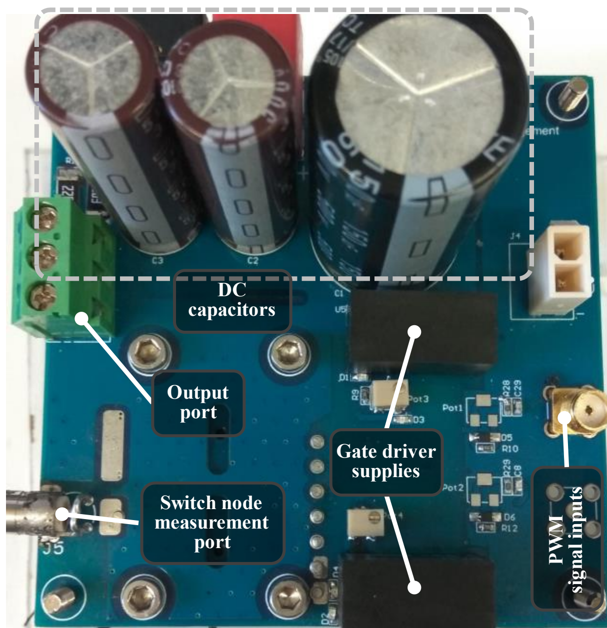
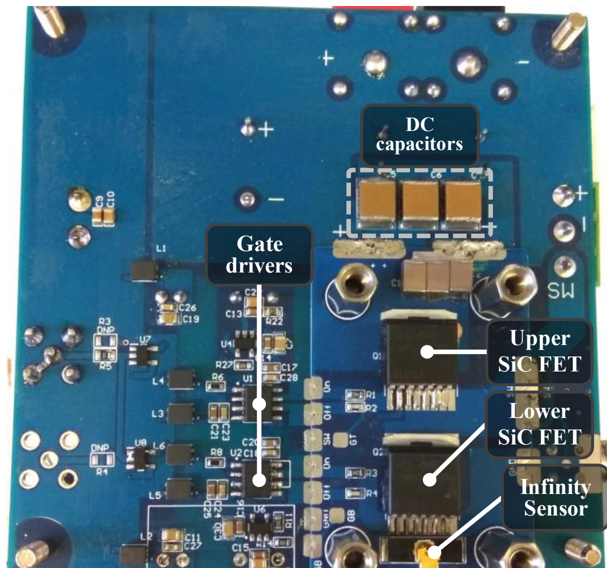


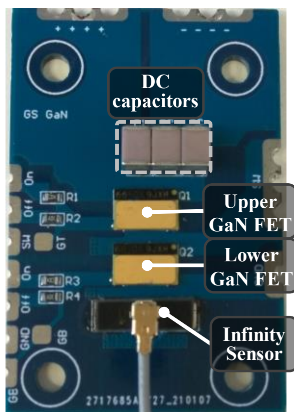
Fig. 3 Experimental setup circuit diagram.



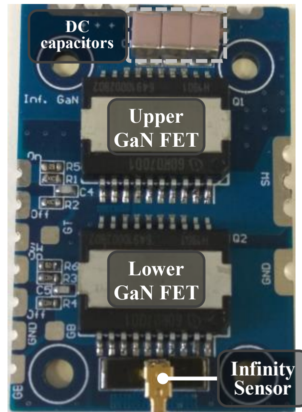
(a) Motherboard topside



(b) Motherboard bottom-side with SiC daughter board attached



(c) Daughter board with GaN Systems devices



(d) Daughter board with Infineon GaN devices

Fig. 4 Test circuit consisting of a motherboard and daughter boards with different devices.

B. *Test Procedures*

The test procedures for the two operating modes are as follows:

Double pulse testing (DPT): A double-pulse control signal, as shown in Fig. 5(a), is constructed such that the turn-on current is 6.8 A. The oscilloscope captures the turn-on edge highlighted in red.

If multiple consecutive double-pulse tests are performed and the captured waveforms averaged together, the measurement fidelity can be increased. A rest time that is long enough to allow the current in the load inductor to decay to zero must be inserted between the consecutive double-pulse sequences.

In view of the dynamic effects of GaN devices, it may be expected that different rest times between double-pulse sequences could influence the switching behaviour. As such, four different double-pulse tests have been performed: one with no averaging and a single sequence, and three with averaging and rest times between repeated sequences of 10, 1, and 0.1 seconds. In all three averaging scenarios, the sequences are repeated 50 times to ensure that switching has evolved towards a repeatable behaviour, with the last ten captured waveforms averaged together.

These four test scenarios are referred to here as: DPT Single, DPT10s, DPT1s, and DPT0.1s.

Continuous operation: With a test circuit without feedback control or protection circuits, care must be taken when starting a continuous-mode test, in order to avoid a large current overshoot in the load. There are two options available:

1. Hold the devices in the off state, activate the DC link, then ramp up the duty cycle of the PWM control pulses from zero to 50%. This type of test is referred to here as "**Continuous (PWM ramp)**"; Fig. 5*(b)*.
2. With the DC link inactive (DC link capacitors discharged and power supply in off/high-impedance state), apply the 50% duty PWM control signal to the GaN devices, then ramp up the DC link, for example by setting the external supply to a low current limit and turning it on, resulting in a steady charging rate of the DC link capacitors. This type of test is referred to here as "**Continuous (DC ramp)**"; Fig. 5*(c)*.

In these tests, the PWM frequency is 100 kHz and the oscilloscope is set to trigger on the five thousandth turn-on switching event, as shown in Fig. 5*(b)* and *(c)*.

For the double-pulse test, an initial pulse duration is used such that the turn-on transition currents are the same in the DPT tests as during continuous-mode operation. Fig. 6 shows the inductor current levels at turn-on switching events. It can be seen that the turn-on current levels are the same for all combinations of DUT and operating mode.

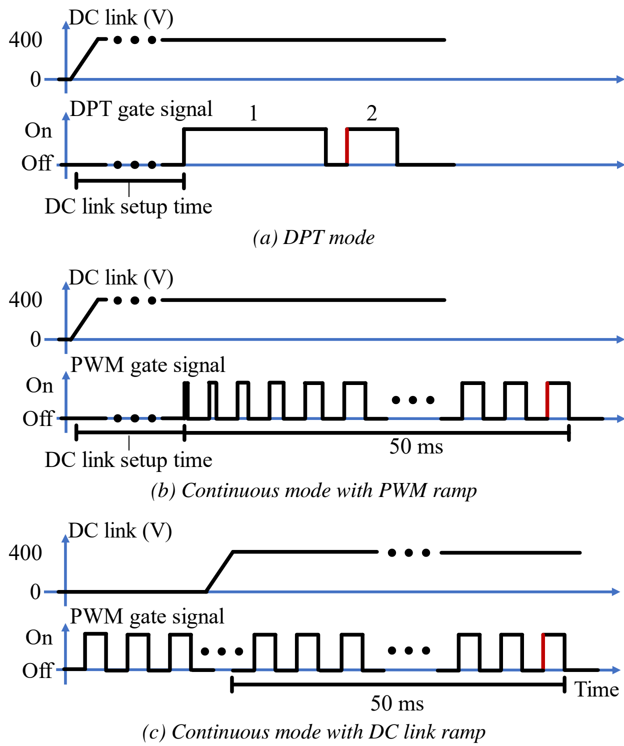


Fig. 5 Gate signal and DC link sequencing for DPT and continuous test modes.

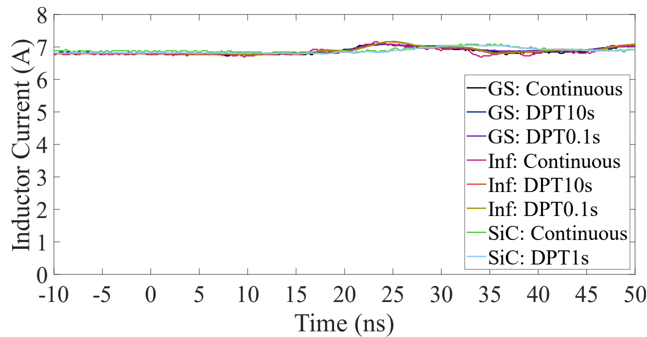


Fig. 6 Turn on current of continuous operation and double-pulse testing with different devices.

C. SiC devices as a control

Fig. 7 shows the measured turn-on switching transition waveforms for continuous-mode operation (with PWM ramp) and the four DPT scenarios, when using the daughterboard that carries the SiC MOSFETs. It can be seen that the results are identical in continuous operation and double pulse testing, and that in this case the rest time between double-pulse events makes no difference, as expected for devices with no dynamic effects.

These data are used as a reference and to show that the discrepancies seen in the GaN device tests are not due to the power converter design or the way the tests are carried out.

IV. Switching Behaviour Mismatch Between Continuous-mode Operation and Double-Pulse Testing

Given the temperature coefficients and dynamic effects of GaN power devices, it may be expected that great care is required to ensure that switching performance in double-pulse testing will actually reflect that seen in continuous-mode operation. The results in this section show that the switching performance in these two operating modes can indeed differ, sometimes significantly so.

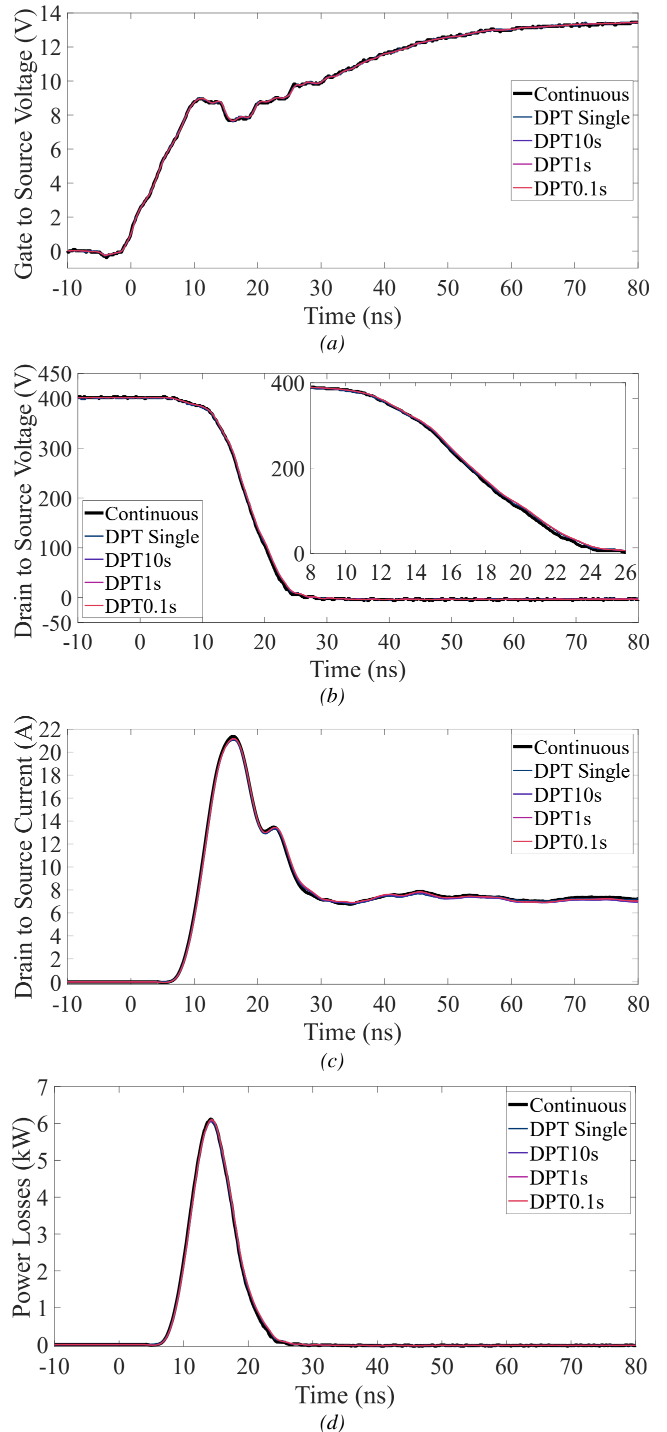
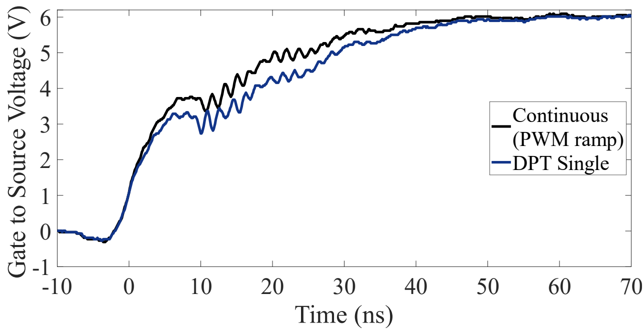
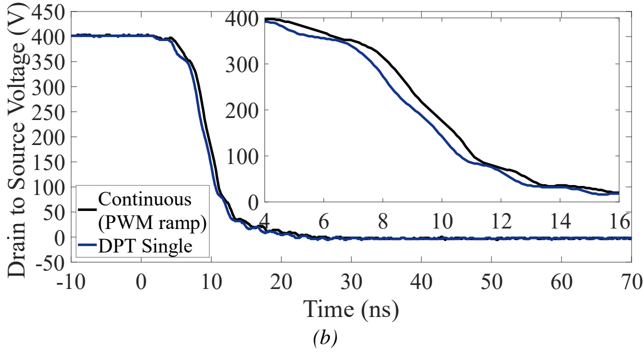


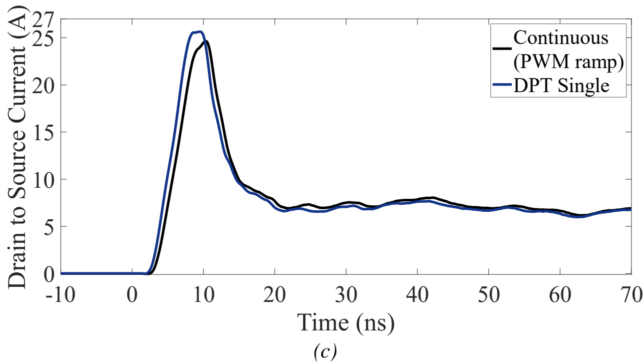
Fig. 7 Measured turn-on waveforms of SiC MOSFETs in continuous mode and double-pulse tests with different rest time. *(a)* Gate to source voltage, *(b)* drain to source voltage, *(c)* drain current, and *(d)* turn-on power losses.

A. Switching behaviour comparison without temperature matching

Fig. 8 and Fig. 9 show the measured turn-on switching events, for Schottky-gate and ohmic-gate devices respectively, in double-pulse and continuous-mode operation (with pwm ramp). Here, the DC-link setup time for the DPT test and the continuous-mode test is more than 100 s. No special measures have been taken to match the device temperature between the two test runs. It can be seen that both







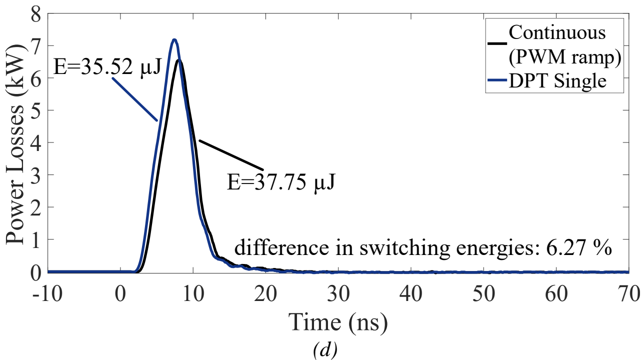


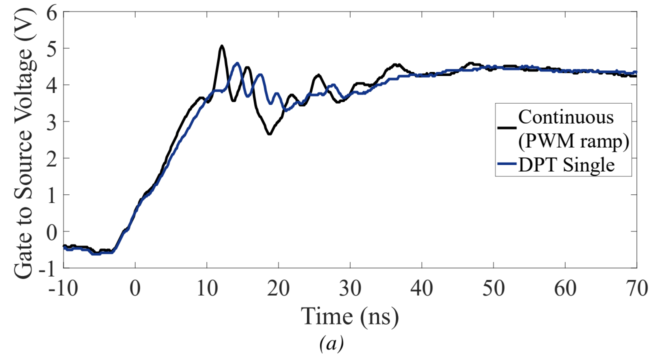
Fig. 8 Measured turn-on waveforms of Schottky-gate GaN devices in continuous mode (with pwm ramp) and double-pulse testing at ambient temperature *(a)* Gate to source voltage, *(b)* drain to source voltage, *(c)* drain current, and *(d)* turn on power losses.

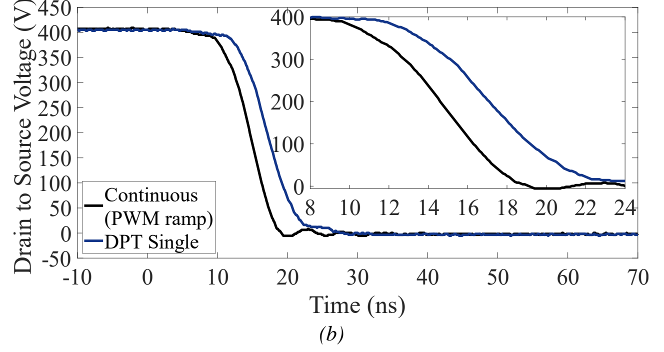
double pulsing and continuous switching produce different results.

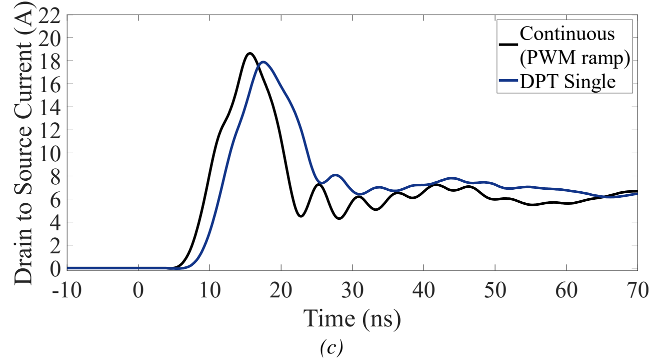
B. Modelling the expected die temperature in double-pulse testing and continous-mode operation scenarios

In order to match the temperature of the devices during the different test scenarios, the temperature rise of the junction must be determined first. Then, the case temperature of the devices during double-pulse testing can be raised to an appropriate level.

Using a manufacturer-supplied thermal model of the GaN Systems device, the simulated junction temperature during the







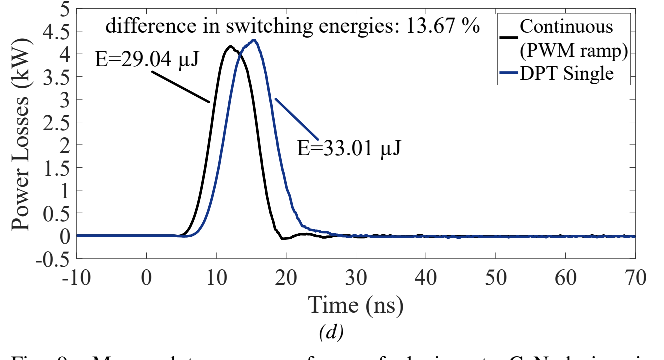
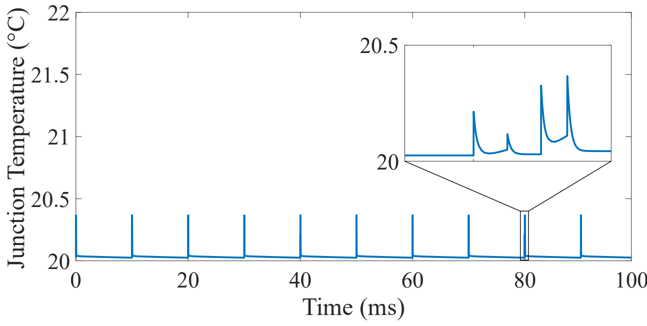
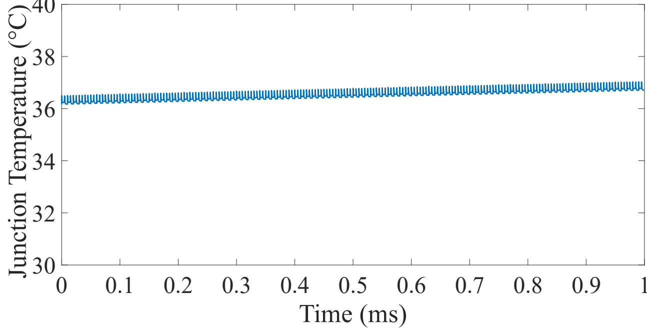


Fig. 9 Measured turn-on waveforms of ohmic gate GaN devices in continuous mode (with pwm ramp) and double-pulse testing at ambient temperature *(a)* Gate to source voltage, *(b)* drain to source voltage, *(c)* drain current, and *(d)* turn on power losses.

pulsed and continuous tests is as shown in Fig. 10. Fig. 10(a) shows the last 12 of 50 double-pulse tests with 10 ms rest time between them, and Fig. 10(b) shows last 1 ms of 50 ms of continuous-mode operation, this being the duration of all continuous-mode tests used here. It can be seen that the junction-temperature change during each switching event is less than 0.5 °C, and the difference in junction temperature from beginning to the end of the double-pulse test is less than 1 °C. As the Infineon devices are larger, they have greater thermal mass, and therefore the expected temperature rise during switching events will be smaller. Infineon do not provide a thermal model for their device; however, as the



(a) Last 12 of 50 double-pulse sequences with a rest time of 10 ms.



(b) 50 ms continuous operation; the data shown is last 1 ms of operation

Fig. 12 Simulated Schottky-gate GaN device junction temperature in different test scenarios.

device is larger, it is expected that the junction to ambient thermal resistance is lower than that of the GaN Systems device and that the junction temperature at the end of the continuous-mode test is less than 37 °C.

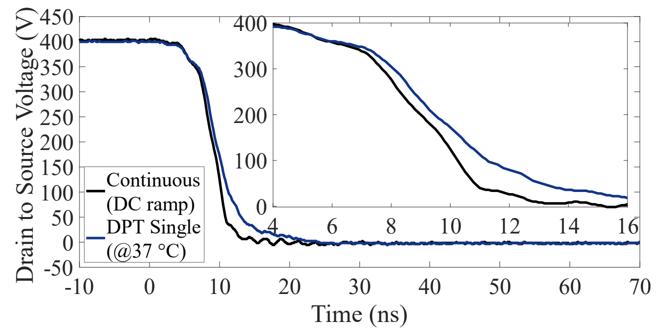
C. *Switching behaviour differences can still be significant, even with temperature-matched tests*

Fig. 11 shows measured turn-on switching events for the Schottky-gate GaN devices in double-pulse and continuous-mode operation (with DC-link ramp). The DC-link setup time for the double-pulse test was more than 100 s. Here, the temperature of the devices was raised to 37 °C in the double-pulse test, by attaching a temperature-controlled heat plate to the devices, so the temperature of the devices is closely matched in the two scenarios. It can be observed that despite the temperature match, the switching behaviour is different in the two scenarios.

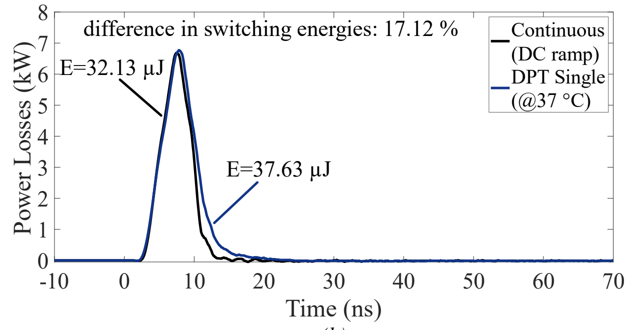
Fig. 12 shows measured turn-on switching events for the ohmic-gate GaN devices in double-pulse and continuous-mode operation (with DC-link ramp). The DC-link setup times for these tests is more than 100 s. Two double-pulse test results are shown: one where the device temperature is at ambient (~20 °C), and another at 37 °C. As the expected junction temperature of the devices during continuous-mode operation lies somewhere between ambient and 37 °C, it can be concluded from these results that if the temperature during the DPT test were to be matched more closely to that during continuous-mode operation, a significant difference in switching behaviour would remain.

V. Matching Double-Pulse Switching to Continuous-Mode Switching

This section demonstrates that for both types of p-gate GaN devices, under specific circumstances, it is possible for pulsed testing of the devices to deliver measured switching performance that matches that seen in continuous-mode operation.

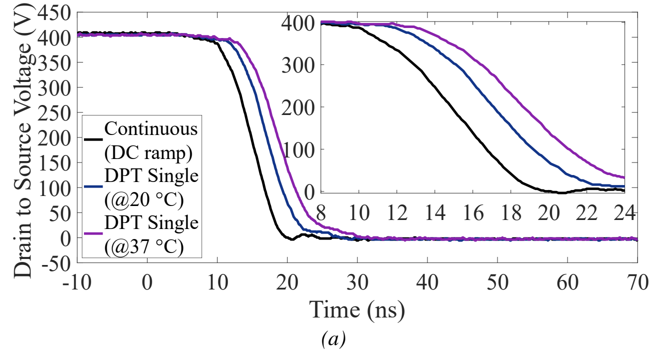


(a)

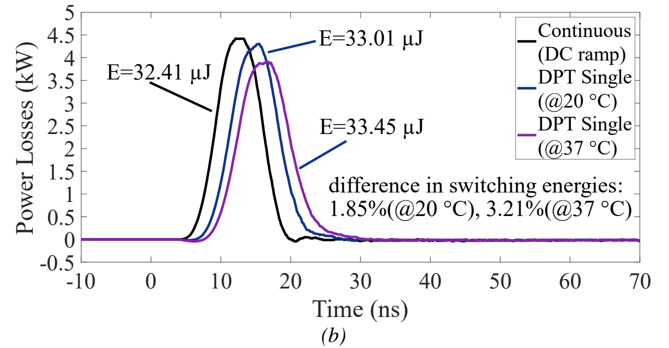


(b)

Fig. 10 Measured turn-on waveforms of Schottky-gate GaN devices in continuous mode (with DC-link ramp) and double-pulse testing at 37 °C *(a)* drain to source voltage, *(b)* turn on power losses.



(a)



(b)

Fig. 11 Measured turn-on waveforms of ohmic gate GaN devices in continuous mode (with DC-link ramp) and double-pulse testing at 20 °C and 37 °C *(a)* drain to source voltage, *(b)* turn on power losses.

A. *Schottky-gate devices*

Fig. 13 shows measured turn-on switching events for the Schottky-gate GaN devices in double-pulse and continuous-mode operation (with PWM ramp). The double-pulse test is repeated with averaging, with a rest time of ten seconds between sequences. The DC-link setup time for both tests is more than 100 s. The temperature of the devices is raised to 37 °C in the double-pulse test.

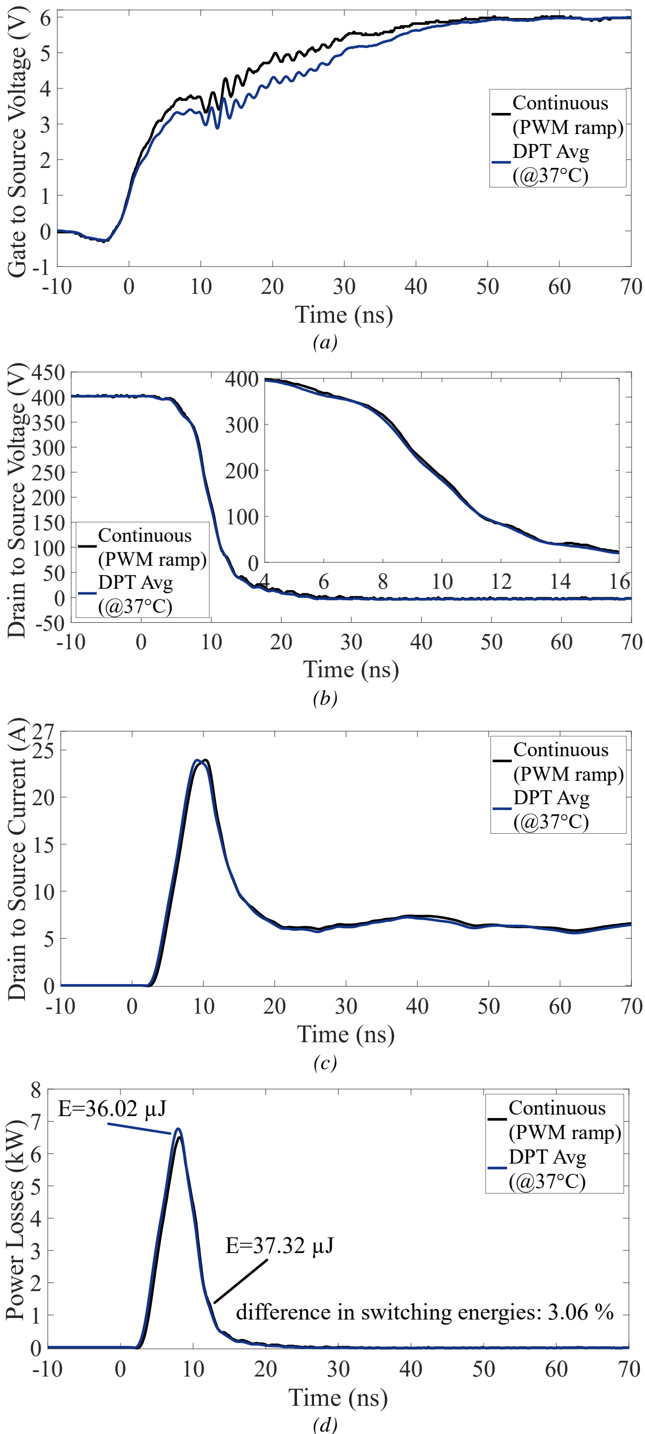


Fig. 13 Measured turn-on waveforms of Schottky-gate GaN devices in continuous mode (with pwm ramp) and double-pulse testing at 37 °C *(a)* Gate to source voltage, *(b)* drain to source voltage, *(c)* drain current, and *(d)* turn on power losses.

B. *Ohmic-gate devices*

For the ohmic-gate devices, no variant of the double-pulse test was found to deliver switching waveforms matching those of the continuous-mode operation. Consequently, this test was extended to an "N-pulse" test method (NPT) which produces results that more closely represent continuous-mode operation.

In this N-pulse sequence, the long initial charging pulse of a traditional double pulse test is split up into N equally-sized pulses, as illustrated in Fig. 14. Hence, double-pulse testing is a subset of N-pulse testing, where N is equal to 2. Based on the number of pulses, the width of the pulses needs to be adjusted so that the current is built up to the required value. Here, the width of the pulses is chosen such that the turn-on

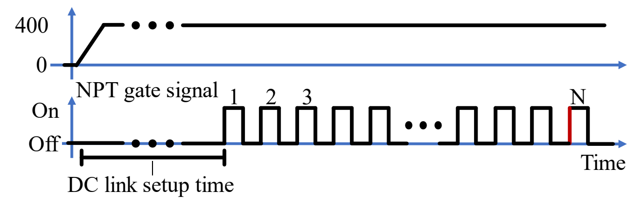


Fig. 14 DC-link sequencing and gate signal for N-pulse test.

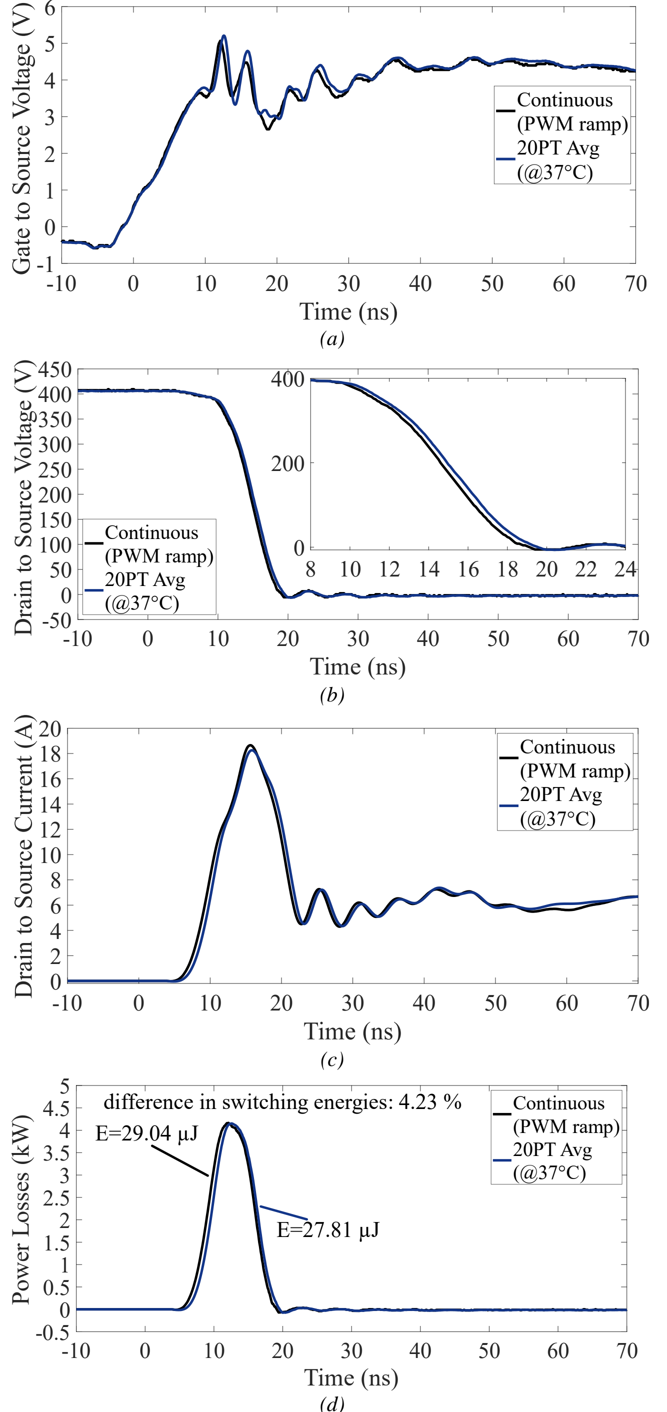


Fig. 15 Measured turn-on waveforms of ohmic-gate GaN devices in continuous and N-pulse testing (NPT) modes at 37 °C. *(a)* Gate to source voltage, *(b)* drain to source voltage, *(c)* drain current, and *(d)* turn on power losses.

current level reaches the same 6.8 A as in the previous tests. Each N-pulse test is run repeatedly, separated by a rest time of 1 s. Once the switching behaviour has settled to a steady state (fifty runs), the oscilloscope captures the last turn-on edge of the switching events, as indicated with a red rising edge in Fig. 14. Results from ten consecutive N-pulse tests are averaged.

The results of using a 20-pulse test, denoted 20PT, with the ohmic-gate GaN devices are shown in Fig. 15; the DC-link setup time for both the tests was more than 100 s. Although these switching waveforms are still not identical, the match is significantly closer than the previously-presented DPT results, and the inferred switching energy matches to within 4%.

VI. Conclusions

Normally-off p-gate GaN devices exhibit significant dynamic effects, where the device history in terms of v_{GS} and v_{DS} biassing can have a strong influence over the switching behaviour of the device. The results in this paper show that, for both types of p-gate GaN devices (Schottky and ohmic), if these effects are ignored when performing a traditional double-pulse test, it is likely to exhibit switching waveforms that do not match those seen in continuous-mode operation. It is also shown that it is possible to find a pulse-testing method that will give a closer match; in this case for Schottky-gate devices repeated double-pulse tests can be used, whilst ohmic-gate devices required the newly-proposed N-pulse test.

Future work will involve a rigorous study of dynamic and temperature effects in these devices, to fully decouple the effects of temperature, and v_{GS} and v_{DS} biassing history. The ultimate aim is to deliver a generalised test solution for a given GaN device, that provides repeatable device switching results, and that accurately represents any given continuous-mode operating condition.

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