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A 1.2 kV 100 kW Four-level ANPC Inverter with SiC Power Modules and Capacitor Voltage Balance for EV Traction Applications

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Abstract—With the recent advances of Silicon Carbide (SiC) power devices and multilevel converter topologies, a combination of them can further push the performance boundaries of electric vehicle (EV) traction inverters while adapting to higher-voltage systems. Prospectively targeting a 1.2 kV dc-link for the next-generation EV powertrain, this paper presents the design and implementation of a 100 kW/1.2 kV three-phase inverter formed by a four-level active neutral point clamped (4L-ANPC) topology and full-SiC power modules. The built converter prototype is the first of its kind (1.2 kV+SiC+4L-ANPC), which is implemented by the commercial half-bridge SiC power modules and enabled by the latest voltage balancing technique based on redundant level modulation. The concept of the converter is validated with a built prototype in a 1 kV/8 kW downscaled rig.

Keywords—multilevel converter, Silicon Carbide, voltage balancing, four-level, electric vehicle

I. INTRODUCTION

Electric Vehicle (EV) applications demand challenging performance improvements of traction drive systems to achieve high power density and high efficiency [1]–[3]. In the past decades, there are two fundamental performance propellers of power converters—Wide Bandgap (WBG) semiconductors and multilevel converters. As the representative WBG technology, Silicon Carbide (SiC) power device has matured in the past years and offers new opportunities to boost the performances of low/medium voltage traction inverters [4], which features ultra-low switching loss, fast switching speed, higher single-device blocking voltage and higher temperature operation. Alongside the advancement of power devices, multilevel converter topologies for low/medium-voltage applications have also been actively explored, such as the Neutral Point Clamped (NPC) converters. Multilevel topologies offer reduced filtering requirements due to lower harmonics and lower switching loss due to lower switching voltage, i.e. a fraction of the full dc-link voltage, compared to conventional two-level converters. Nowadays, new multilevel topologies with more voltage levels (e.g. four levels or more) are still actively being proposed [5] to cope with the trend of higher voltage and higher power systems. As studied in the scaling law for multilevel converters in [6], while increasing dc-link voltage, more voltage levels are required to counter the impact on converter performance caused by the higher switching voltage and switching losses. The pursuit of a higher number of voltage levels is also driven by

further reduction of dv/dt , electro-magnetic interference (EMI) and filtering requirement.

In recent years, upgrading the dc-link voltage from 400 V to 800 V has been a trend for the new-generation EV powertrain systems [7]–[12] to accommodate the increased power demand and performance requirements, which has been adopted by car manufacturers such as Porsche and Fisker [12]. Comparing with the 400 V system, the 800 V powertrain architecture can increase the power density, reduce weights and reduce battery charging times [7], [11]. More specifically, with the same power level, increasing the voltage results in reduced phase current, which leads to the reduction of the cross-section of the wiring harness and subsequently the reduced amount of copper required in the system. A higher dc-link voltage can also lead to a higher density of the motors and enables the extreme fast chargers (XFC) [9], [10]. Although, a higher dc-link voltage also brings challenges such as the dv/dt issues, insulation and partial discharge issues and battery safety concerns [9], [10].

With the development of SiC devices and multilevel topologies, it can be expected that the EV system voltage could further scale up to further improve the system performance and capacity [2], [8]–[13]. As shown in [10], upgrading the dc-link voltage from 400 V to 1.2 kV can reduce the weight of copper by 63% for the electric harness inside a 150 kW EV system, which is an additional 30% improvement compared to an 800 V system. Additionally, considering a 350 kW charger, a dc-link of > 1 kV can ensure the charging cable's weight within the safety standards (e.g. 22.7 kg for a single person to handle [10]).

Considering the common 400 V two-level system as the baseline, an 800 V three-level configuration (e.g. [9], [14], [15]) and a 1.2 kV four-level configuration will maintain the same switching voltage of 400 V and dv/dt . Therefore, a four-level converter seems to be a good solution to scale up the dc-link voltage to 1.2 kV for EV systems. Among the four-level dc/ac converter topologies, the four-level active NPC topology (4L-ANPC, [16], [17]) enjoys the fewest number of devices, which can be considered as the most “simplified” four-level topology. Topology simplification is an effective way to reduce the number of devices of multilevel converters and subsequently reduce the cost, complexity and volume/weight [5]. Thanks to the simplified and “fractal” structure, a 4L-ANPC phase leg can be formed by three mainstream two-level power modules without any clamping diodes or bi-directional switches, which overcomes the difficulty of lacking available multilevel power modules [10].

Fig. 1. Simplification of four-level topologies (a) 4L-HC (b) middle state of simplification (c) 4L-ANPC [5]

However, as the penalty, the topology simplification commonly leads to a higher blocking voltage requirement of part of the devices and increased difficulties in balancing the capacitor voltages. For example, simplified from the four-level hybrid clamped (4L-HC) converter [18], the 4L-ANPC topology has two devices (red devices in Fig. 1(c)) with their blocking voltage increased from 33% to 66% of dc-link voltage. Additionally, while 4L-HC has the self-balancing capability, 4L-ANPC features an increasingly challenging voltage balancing issue that cannot be completely solved by the conventional approaches [19], [20]. Therefore, the 4L-ANPC topology has not been commonly applied in single-end inverters. Although this topology has been patented and commercialized by Schneider Electric [21], it needs auxiliary “dc bus balancers” to maintain the three dc-link capacitor voltages. As the latest advance, Redundant Level Modulation (RLM) [22] and similar approaches [23] have been brought up to solve its voltage balancing issue without introducing auxiliary circuits, which lift this obstacle that hinders the wider application of this topology. However, these modulation-based voltage balancing methods mandatorily utilize redundant output voltage levels and require an increased number of switching events (e.g. up to +100 % [22]) as the penalty of gaining extra controllability, which significantly increases the switching loss and undermines the benefit as a multilevel topology. Fortunately, SiC devices bring new opportunities for these multilevel topologies because of their higher single-device blocking voltage (e.g. 10+ kV in SiC MOSFETs in contrast to 6.6 kV in Si IGBTs) [24] and significantly lower switching losses. These two features of SiC devices exactly counter the two weaknesses mentioned above in simplified topologies.

Therefore, the motivation of this work is to combine the SiC devices and the four-level multilevel topology as a solution of traction inverter for an EV powertrain with a prospective 1.2 kV dc-link. The contribution of this paper is the design and implementation of a 100 kW inverter with 4L-ANPC topology and full-SiC power modules. This inverter is the first of its kind (1.2 kV + SiC + 4L-ANPC), which is enabled by the latest commercial half-bridge SiC power modules and advanced redundant level modulation for voltage balancing control of this topology. The design, implementation and performance analysis will be presented in the rest of this paper. A prototype is built and tested in a downscaled rig as proof of concept.

II. TOP-LEVEL DESIGN AND OPERATION OF THE INVERTER

Fig. 2 shows the four-level ANPC topology under consideration. Compared to the three-level ANPC topology [5],

this topology has the same number of power devices, i.e. six devices per phase, while it outputs one additional power level to further reduce the dv/dt and switching losses. As another practical advantage, these six switches can be formed by three half-bridge power modules. The operation of the four-level converter is illustrated in Fig. 3, which outputs four voltage levels to synthesis the fundamental-frequency output voltage.

Fig. 2. Configuration of a 4L-ANPC converter.

Fig. 3. Operation of a four-level NPC converter.

A. Power Devices

As mentioned in the introduction, S2 and S2' need to block a higher voltage in the 1.2 kV system (800 V instead of 400 V). However, the actual devices for S2 and S2' do not need to have a significantly larger voltage safety margin because this higher voltage is a static blocking voltage requirement and the actual switching voltage is still one-third of the dc-link, i.e. 400 V. As a common practice, the selection of power device typically considers a 100% margin on the switching voltage (400 V) to account for the voltage overshoot and a 20% margin on the static blocking voltage (800 V) for safety. In this case, a 1.7 kV rated power device provides an abundant margin for S2 and S2', which leaves a margin of +325% to the 400 V switching voltage and +112% to the 800 V static blocking voltage. And 1.2 kV

TABLE I PARAMETERS OF THE SELECTED POWER DEVICES ($T_j = 150^\circ\text{C}$)

Voltage rating	Current rating	Power module		V_{FW0} (V)	R_{on} (m Ω)	V_{FW} (V) @ 300 A	E_{sw} (mJ) (600 V, 300 A)	R_{th_jc} $^\circ\text{C/W}$
SiC	300 A	CAS300M12BM2	MOSFET	0	7.7	2.31	5.8 (ON) + 6.1 (OFF)	0.070
			Diode	0.75	4.2	2.0	0	0.073
		CAS300M17BM2	MOSFET	0	16.2	4.86	8.7 (ON) + 6.6 (OFF)	0.067
			Diode	0.75	4.8	2.2	0	0.060

rated power devices are sufficient for Module 1/3. As the matured commercial SiC modules from Wolfspeed, the 1.7 kV module CAS300M17BM2 and the 1.2 kV module CAS300M12BM2 are selected for Module 2 and Module 1/3 in, respectively. Taken from the datasheet, the parameters of the selected SiC power modules are listed in Table I. This configuration can practically allow a dc-link voltage of up to 1.8 kV. In comparison, a 1.2-1.5 kV system with a two-level topology will require 2.5 kV SiC power devices [25] that are not commonly available yet.

B. DC-link Capacitor Voltage Balancing

The common dc-link is formed by three capacitors C1, C2 and C3 in series. As established in [20], [22], this topology as a single-end inverter will lose the voltage of the middle capacitor (i.e. fully discharge) with conventional modulation approaches in which only two voltage levels are used in one carrier cycle as shown in Fig. 4(a). However, if a third voltage level is allowed, as shown in Fig. 4(b), the voltage balancing problem/limitation can be completely resolved. This third voltage level is the “redundant level” that is redundant for synthesising the reference voltage in a switching cycle, but it can bring a new degree of freedom for voltage balancing, which is the core concept of the redundant level modulation (RLM) [22].

Fig. 4. Illustration of output voltage pattern in one carrier cycle with an equal volt-second product (a) conventional (b) redundant level modulation (0, 1, 2 represent three voltage levels)

As the basic principle, the RLM alters the high-frequency output voltage on a switching cycle basis without altering the synthesized fundamental-frequency voltage. In other words, the width of the three voltage levels in Fig. 4(b) can be adjusted according to the imbalance of the capacitor voltage while the average output voltage (volt-second product) of the switching cycle remains the same, which is achieved by introducing an offset of duty ratio ΔD

$$\begin{cases} D'_4 = D_4 + \Delta D \\ D'_3 = D_3 - 2\Delta D \quad (U_{ref} \geq 0) \\ D'_2 = \Delta D \end{cases} \quad (1)$$

$$\begin{cases} D'_3 = \Delta D \\ D'_2 = D_2 - 2\Delta D \quad (U_{ref} < 0) \\ D'_1 = D_1 + \Delta D \end{cases}$$

where D_4, D_3, D_2, D_1 are the original duty ratios of the four voltage levels derived from regular modulation; D'_4, D'_3, D'_2, D'_1 are the altered duty ratios obtained from RLM; U_{ref} is the reference voltage of a switching cycle. This duty ratio offset ΔD introduces one additional voltage level (e.g. level 2 when $U_{ref} \geq 0$ and level 3 when $U_{ref} < 0$). The altered duty ratios (D'_3 and D'_2) can lead to the manipulation of the C2 voltage in one switching cycle as

$$\Delta U_{C2} = \frac{1}{3 \cdot C \cdot f_{sw}} \cdot \sum i_x (D'_{2x} - D'_{3x}) \quad (2)$$

where C is the capacitance of each capacitor in series; x represents the phase denotes ($x = a, b, c, \dots$); i is the load current.

Based on the RLM concept, a closed-loop voltage balancing scheme has been developed and presented in [22], which is simple-to-implement through level-shifted carriers and free from PI controllers. As illustrated in Fig. 5, the RLM pattern can dynamically reduce the red discharging area and increase the blue charging area for C2 while maintaining the equal volt-second product of each carrier cycle, which gains a wider controllable margin of the capacitor voltages than the limited conventional approach (e.g. [20]). The offset duty ratio ΔD is calculated in each switching cycle through (1)(2) based on the measured voltage imbalance of the capacitors.

Fig. 5. Illustration of redundant level modulation (RLM) implemented in a four-level NPC converter [22]

As verified in [22], this voltage balancing control is effective even when the fundamental frequency is low (e.g. $f_0 = 1$ Hz), because the balancing is achieved on a switching cycle basis. This RLM scheme also extends the operation range of the 4L-ANPC topology to the full span of modulation indexes ($M = 0 \sim 1.15$) and power factors ($\cos\phi = 0 \sim 1$) without losing the voltage balance of dc-link capacitors. More details of this control scheme can be found in [22]. The harmonic performance of the converter is also evaluated in simulation, which yields 41% THD on the output line voltage with no low-frequency harmonics and the largest high-frequency harmonic of 20 % of the fundamental component at $2f_{sw}$.

Considering the practical implementation of the proposed inverter, the additional switching events (e.g. +100%) and the additional switching losses induced by the RLM operation should be considered mandatory and accounted for in the estimation of efficiency and design of the thermal components.

The dc-link capacitances are sized at $C1 = C2 = C3 = 150 \mu\text{F}$ assuming film capacitors for EV applications. In this case, the high-frequency dc-link capacitor voltage ripple is below 2% of dc-link voltage as evaluated in the simulation.

C. Power Loss Evaluation and Thermal Design

To perform the thermal design, firstly the converter power loss and efficiency are evaluated in Simulink/PLECS based on the data in the manufacturer datasheet, assuming the junction temperature is at 150°C . With the synchronous conduction implemented, the power losses of the devices are predicted as visualized in Fig. 6. As the drawback of the 4L-ANPC topology, the majority of the power loss concentrates in the two outer devices [17], i.e. the Module 2 with a 1.7 kV rating, which accounts for 65% of converter loss in the analyzed case. This imbalance of power loss between power modules leads to an uneven thermal distribution that needs to be taken into account in the thermal design.

Operating at 100 kW and 1.2 kV, the designed converter can still maintain a 99.4% efficiency at 5 kHz of switching frequency f_{sw} , as benefited from the multilevel topology (lower switching voltage) and low switching loss of SiC MOSFETs. Note that this result already included the effect of increased switching events caused by the redundant level modulation [22] to balance the capacitor voltages. When the switching frequency f_{sw} is increased to 50 kHz, the converter can still keep the efficiency above 98% with 100 kW output. When the output power is increased to 200 kW, the converter can still offer a > 97.5% efficiency up to 50 kHz.

Fig. 6. Estimated converter power loss (a) breakdown at $f_{sw} = 5 \text{ kHz}$ (b) efficiency vs. f_{sw} .

With the power losses estimated, the required thermal resistance of the heatsink is retrieved from the simplified thermal network model shown in Fig. 7(a), where $R_{th_{jc}}$ is the junction-to-case, $R_{th_{cs}}$ is the case-to-heatsink and $R_{th_{sa}}$ is the required heatsink-to-ambient thermal resistance. With the $R_{th_{jc}}$ given in the datasheet as 0.075, $R_{th_{cs}}$ assumed as 0.025 and $T_{j_{max}}$ assumed at 120°C , the maximum $R_{th_{sa}}$ of the heatsink is estimated against the carrier frequency as shown in Fig. 7(b). Depending on the application, if the ambient temperature is 25°C , the presented converter prototype can be mounted on an air-cooled heatsink even up to 50 kHz (where the required $R_{th_{sa}}$ is

0.138°C/W), thanks to the low losses of the presented SiC + 4L-ANPC configuration. If the application is assumed to be in an EV with the coolant ambient at 90°C , the $R_{th_{sa}}$ ranges between $0.108\sim 0.017^\circ\text{C/W}$ from 5 kHz to 50 kHz, which typically requires liquid-cooled cold plates.

Fig. 7. Thermal design (a) thermal network model for power modules (b) required thermal resistance

To further inform the thermal performance of the proposed converter, the junction-to-coolant temperature rise is evaluated with the assumption that it is mounted on commercial coldplates (e.g. $R_{th_{sa}} = 0.008^\circ\text{C/W}$ [26]). The results are presented in Fig. 8 showing only S1, S1' and S2 due to the symmetry of the topology. The junction temperature of the outer switch S2 is the limitation due to the concentrated loss. In this case, the proposed converter can still sustain a continuous 200 kW output and 30 kHz switching frequency with a coolant temperature of 65°C [27] to keep the S2 junction temperature below 125°C .

Fig. 8. Junction-to-coolant temperature rise ($R_{th_{sa}} = 0.008^\circ\text{C/W}$)

III. PROTOTYPE IMPLEMENTATION

A. Busbars

Considering the fast switching speed and high dv/dt of the SiC devices, low-inductance interconnections between the dc-link capacitors and power modules are formed by 4-layer laminated copper busbars, which also ensures short commutation loops [28].

In the four-level structure, the mid-point of each power module is susceptible to excessive ringing during a switching transition if the parasitic inductance in the circuit layout is too high. Thus, to avoid this, the module layout and the busbar interconnects for the structure were designed to minimize the parasitic inductance as much as possible. The four-level structure has 3 switch nodes, one at the mid-point of each

module, resulting in 3 critical loops, shown in Fig. 9, around which the parasitic inductance and capacitance should be kept to a minimum. As the connections between each switching device pair are internal to each module, the parasitics inductance can only be reduced between the modules and the DC-link capacitors. Film capacitors are used for the dc-link because of their low ESR/ESL and high reliability for EV applications.

Fig. 9. DC-link design of the prototype (a) critical loops (b) busbar connections

For each phase, the modules and DC-link capacitors were arranged as shown in Fig. 10 to minimize the distance between the common connection points in the phase.

Fig. 10. Module and DC-link capacitor arrangement for single phase

This layout is repeated for each phase as shown in Fig. 11.

Fig. 11. Module and DC-link capacitor arrangement, 3-phase structure

To further reduce the parasitic inductance, multi-layer planar busbars were designed. Two unique busbar designs were constructed: a 2-layer planar busbar for the connections between module 2 and the mid-point of modules 1 and 3, and a 4-layer planar busbar for between the DC-link capacitors and modules 1 and 3, as shown in Fig. 9(b). Separate 2-layer busbars are used from each phase, while a single 4-layer busbar is shared between the 3 phases. The layers were made from 0.45 mm copper sheets and were insulated from each other with Dupont Nomex 410 insulation paper, typically used as machine slot liner material. The insulation extends beyond the edges of the copper plates so that voltage clearance and creepage meet the system voltage rating of 1.2 kV. The exploded views of the 2-layer and 4-layer planar busbars are shown in Fig. 12. The complete busbar arrangement is shown in Fig. 14. The selected dc-link capacitors are 3x3 WIMA DCP4 series film capacitors rated 600 V, 50 μ F.

Fig. 12. Busbar construction (a) 2-layer inter-module connection (b) 4-layer dc-link busbar

B. Gate Driver

This prototype employs commercial gate driver cores, 2SC0650P from Power Integrations Inc., with dedicated adapter boards to form a low-profile and low-driver-loop modular unit for each power module, which is shown in Fig. 13. The gate driver is tuned to drive the SiC devices with a +15 V dc supply, -5/+20V output and 3.25 Ω external gate resistance. The adapter board is designed with clearances for the M6 screw caps to pass through so that the gate driver unit can be closely placed on top of the busbars and the power modules to minimize the gate driving loop.

Fig. 13. Customized low-profile gate driver units

(a)

(b)

Fig. 14. Four-level prototype including modules, DC-link capacitors and planar busbars (a) rendered design mounted on a coldplate (b) the built prototype with air-cooled heatsink

C. Features of the Prototype and Potential Improvements

Apart from the low switching loss of SiC power devices, the main benefit of the proposed converter comes from the four-level structure to accommodate the 1.2 kV dc-link voltage. Firstly, the voltage step between every two layers of the laminated busbar and between every two levels of the output voltage is only 400 volts, which eases the partial discharge and insulation concerns on the busbars [29] and motor winding insulation [4] comparing to a two-level 800 V system. The four-level operation also leads to the power devices only switching at 400 V, rather than the full dc-link voltage of 1.2 kV, which eases the harsh requirement of the dc-link parasitic inductance comparing to the case of a two-level converter [30], [31] considering the high dv/dt of SiC devices. Additionally, the 400 V voltage step also results in a lower requirement for the dc-link capacitors and voltage sensors. In the prototype, the film capacitors and LV-25P voltage sensors are designed with only 600 V rating, rather than the full 1.2 kV, to leave a +50% margin. Given the selected voltage ratings of the devices in Table I, the selected power module configuration can allow a dc-link voltage up to 1.8 kV. In that case, the switching voltage becomes 600 V.

The dimensions of the converter sitting on an air-cooled heatsink are 420*210*120 mm, which leads to a power density of 9.3 kW/L at 100 kW. Changing to a cold plate with a thickness of 20 mm [26] and the same mounting area, the converter power density can reach 18.7 kW/L (420*210*60 mm), excluding the external coolant circulation system. Considering the 300 A current rating of the power modules, this converter configuration can be further pushed up to 200 kW output with a 1.2 kV dc-link as evaluated in Section II.C without overheating. In this case, the power density of this converter can reach 37.34 kW/L.

The power density can be improved by replacing the power modules in the regular 62mm package with a more low-profile package, such as the CAS325M12HM2 from Wolfspeed [14], which reduces the height of the power modules from 30 mm to 16.8 mm. Although CAS325M12HM2 only has a 1.2 kV voltage rating, it is sufficient for the proposed 1.2 kV system as analysed in Section II.A. Additionally, as can be seen from Table I, the conduction characteristic of the 1.7 kV power module is relatively undesirable, which has a $R_{ds, on}$ of 16.2 m Ω at 150 °C. This power module is the main thermal limitation of the 4L-ANPC configuration when the load current/power level

increases as evaluated in Fig. 8. By replacing CAS300M17BM2 with CAS325M12HM2, which has a $R_{ds, on}$ of 7.5 m Ω at 150 °C, the conduction loss can be significantly improved, especially in the case with a higher current. Moreover, CAS325M12HM2 allows a junction/case temperature of 175 °C, rather than 125 °C, which will enable a higher-temperature operation and more compact mechanical design due to a wider margin of temperature rise.

IV. EXPERIMENTAL VALIDATION

The demonstrator is tested in a downscaled 1 kV/8 kW rig for proof of concept, with the specifications listed below.

TABLE II TEST RIG SPECIFICATIONS AND COMPONENTS

DC-link voltage and supply	1 kV, EA-PS 81000-30 3U
Output power/current	8 kW/9 A rms
Carrier frequency f_{sw}	5 ~ 50 kHz
Fundamental frequency f_0	50 Hz
Differential voltage probe	Pico TA042
Current probe	Keysight N2783A
Current sensor	LEM LA55-P
Voltage sensor	LEM LV25-P
R	33 Ω , 3 kW per phase
L	6.3 mH per phase

Fig. 15 shows a picture of the test rig with the prototype mounted on a forced-air-cooled heatsink and wired up with load and gate signals. As evaluated in the last section, this configuration and power level only requires an air-cooled heatsink.

Fig. 15. Downscaled test rig (load R, control board and dc supply are outside the photo)

Running at 1 kV dc-link voltage, Fig. 16 shows the captured phase voltage, line voltage, and output current of the converter. With the RLM voltage balancing [22] implemented, it can be seen in the phase voltage that the converter steadily outputs four voltage levels, which means the capacitor voltages are all well balanced at one-third of the dc-link voltage (i.e. 333.3V). The output line voltage shows seven voltage levels, and the output current is sinusoidal without any visible low-frequency distortions. Fig. 17 shows a zoomed-in view of the waveforms. With the time per division set at 100 μ s, two divisions equal to one switching cycle ($f_{sw} = 5$ kHz) in this screenshot. As can be seen, the converter outputs the RLM voltage pattern with three voltage levels and four switching transitions in each shown carrier cycle, which is intended as shown in Fig. 4(b). The main side effect of this operation, the increased switching loss, is mitigated by the SiC devices.

Thanks to the closed-loop RLM scheme, the challenging voltage balancing issue is successfully solved in this topology. The converter in this case is operating at a high modulation index ($M = 0.9$) and a high power factor ($\cos \varphi = 0.99$) in this case, which is close to the worst-case scenario for capacitor balancing in this topology. Note if a conventional voltage balancing scheme is applied instead of RLM (e.g. the ones based on zero-sequence signal injection or redundant vector [20]), the middle capacitor C2 will fully discharge in this case and the single-end inverter will not be able to output four voltage levels.

Fig. 16. Experimental waveforms with 1 kV input voltage and 8 kW output (phase voltage u_b referenced to the negative dc rail)

Fig. 17. RLM pattern of the output voltage

Fig. 18 is the further zoomed-in waveforms showing the switching transitions when the output voltage level steps. Thanks to the four-level topology, the output voltage has a step of 333.3 V rather than the full dc-link voltage of 1 kV. As a result of the low-inductance laminated busbars for the power loops, the voltage overshoot of the shown step is around only 100 V, which is 30 % of the switching voltage and 10% of the dc-link voltage, despite the fast switching of the SiC MOSFETs.

Fig. 18. Switching transitions of output voltage

V. CONCLUSION

This paper presented the design and implementation of a 1.2 kV/100 kW inverter formed by full-SiC power devices and 4L-ANPC topology, which is implemented with commercial half-bridge SiC power modules and enabled by the latest voltage balancing technique, i.e. redundant level modulation. The proposed inverter features very high efficiency (e.g. 99.4% at $f_{sw} = 5$ kHz and 100 kW) in the prospective 1.2 kV dc-link system as benefited from the SiC devices and multilevel topology. A proof-of-concept prototype is built and tested in a downscaled (1 kV/8 kW) test rig with forced-air-cooled heatsinks. The proposed inverter configuration is a prospective solution for the next-generation electric vehicle powertrain systems with kilovolt level of dc-link voltage (e.g. 1.2 kV).

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