Analysis of cyclic spontaneous switchings in GaN & SiC cascodes by snappy turn-off currents


Abstract – This paper investigates the crosstalk-induced spontaneous switchings as continuous cycles of turn-on and turn-off transients as a key reliability criterion in SiC and GaN cascode power devices. The paper presents a wide range of measurements to describe the severity of unwanted switching cycles in presence of a few diodes with high turn-off dI/dt which results in a negative gate voltage induced by the source inductance. Modelling is performed which confirms the theory described to explain the root cause of the continued oscillatory transients and comparisons are made with standalone SiC power MOSFETs.

1. Introduction

Wide-bandgap power semiconductor devices are the enabler technology of today’s power electronics. Gallium Nitride (GaN) high electron mobility transistors (HEMTs) and Silicon Carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs) are the key device structures that have enabled taking advantage of the wide-bandgap properties of these devices [1]. These enable fast transients and reduced switching and conduction losses. As a result, these characteristics lead to smaller passive components (as switching at higher frequencies is possible) and less thermal management ancillary requirements. Overall, compact converters will become possible at reduced size, weight and cost.

However, driving these devices also have limitations. The gate oxide interface of Silicon Carbide power MOSFETs is prone to failures, especially at higher temperatures and when the device is blocking high voltages instigating high electric fields at the epitaxial region edges. This is due to the presence of carbon atoms in SiC during its oxidation process and will take place regardless of whether the oxidation process is wet (in presence of water) or dry (only with oxygen). The wet oxidation process is more effective and faster, but it will also create other defects due presence of hydrogen. These defects will lead to charge trapping, and in turn shift of the threshold voltage with catastrophic consequences especially when the devices are operating in parallel. This also limits the possible negative voltage range on the gate. The GaN HEMTs are lateral devices with a two-dimensional electron gas layer at the heterojunction of GaN and AlGaN regions. This structure is formed by the difference of the fermi-level of the two regions, and leads to a low threshold voltage and low gate voltage capability. To put this into context, SiC MOSFETs have typically 20 volts gate voltage limit with a threshold of 2.5 V while GaN HEMTs have a voltage limit of only 6 volts with thresholds as low as 1 V.

The aforementioned issues have led to development of a new topology of transistors as cascodes of an enhancement-mode low-voltage silicon MOSFET coupled with a normally-on SiC JFET or GaN HEMT. This structure enables taking advantage of high blocking voltage of the wide-bandgap semiconductors, coupled with fast switching rate enabled by the small parasitic capacitances of the driving silicon MOSFET. Therefore, the gate oxide failures in SiC MOSFET is avoided, and the threshold voltage in GaN transistor is in effect increased.

However, the fast transients in SiC and GaN cascodes can lead to unwanted switching events. The existing reports [2] explain this as crosstalk which is the unwanted turn-on of the transistors due to the significant dV/dt on its Miller capacitance, which induces a current on its gate resistance. This generates a voltage on the gate which can lead to unwanted turn-on of the transistor if it is larger than its threshold voltage. Literature have commonly studied this self-turn-on phenomenon in a double pulse tester [3, 4]. The impact of unipolar & bipolar gate drivers on elimination of the crosstalk voltage is also analysed [5].

In this paper, it is shown that GaN & SiC cascodes not only suffer from the self-turn-on characteristics, but in fact they may experience significant self-turn-off transients, especially where the device is switching a negative current with high dI/dt into the source inductance of packaging. The characteristics of this phenomenon is emulated by using a SiC Schottky Barrier Diode (SBD) and the body diode of the same device under test (DUT) [6]. The double-pulse switching circuit is shown in Fig.1. The devices under test are UnitedSiC’s SiC Cascode with reference UJ3C065080K3S rated at 650V & 23A at 100°C, and Transphorm’s GaN cascode referenced TP65H050WS with similar ratings of 650V & 23A at 100°C. For the sake of comparison, Wolfspeed’s SiC MOSFET with reference C2M0160120D is also tested. Section 2 discuss the experimental measurements, section 3 will demonstrate a sample of the modelling performed while section 4 concludes this synopsis.

2. Experimental measurements

A wide range of measurements are performed in different switching rates adjusted by gate resistances. It can be seen in Fig.2 that very high dI/dt results in high negative voltage peaks induced on the gate of the switching transistors by the source inductance which leads to spontaneously turn-off of the transistor while it is transitioning to turn-on stage.

The continuation of applying a positive gate voltage to the gate of the transistor by the gate driver and the negative gate voltages induced upon switching with low gate resistances leads the transistor to enter an oscillatory loop of turn-on & off transients

Fig. 2. The gate voltage overshoots on the source inductance by the high snappy dI/dt results in spontaneous unwanted turn-off of the transistor during its turn-on transient and continuous gate bouncing.
as gate bouncing issue. This, as shown in Fig.3 can lead to failure of the transistors at low gate resistances, which in this case has resulted in a short-circuit into the transistor and current rise until the DC-link capacitors are fully discharged [7-9].

The aforementioned cyclic switching behaviours are shown in Fig.4 for the SiC & GaN cascodes alongside SiC MOSFET device. The first two graphs show turn-on waveforms of gate voltage and the drain current for SiC MOSFET with $R_G$ of 4.7 $\Omega$ and 100 $\Omega$. The device transients with 4.7 $\Omega$ exhibit significant gate voltage spikes while it is reduced when the gate resistance is increased to 100 $\Omega$. As for the SiC cascode transistor in middle, the transients demonstrate a similar trend but with more oscillations. The last row of figures exhibit the same measurements for the GaN cascode which has the highest rate of switching transients. The measurements indicate very severe continuous ringing when switched at low gate resistances and the devices does not reach steady-state even in 2$\mu$s. As the gate resistance is increased, the device still exhibits some oscillations, but it eventually reaches the steady-state. In short unwanted cyclic turn-on & off transients are less pronounced in the SiC MOSFET (as it has the largest input capacitance and internal gate resistance), followed by the SiC cascode device while it is the worst in the GaN cascode transistor, due to the fact that in cascodes the switching MOSFET is only rated at about 20 volts which results in very small parasitics, while the normally-on HEMTs switch a tenfold faster than SiC JFETs due to their lateral two-dimensional electron gas layer resulting in very small parasitic.

The free-wheeling diode (FWD) for measurements of Fig.4 were performed by using the MOSFET body diodes which have considerable reverse recovery charge. To rule out the role of the recovery charge and its snappiness measurements are repeated by using a SiC Schottky barrier diode (SBD) as the FWD. The results are shown in Fig.5. It can be seen that when $R_G$ of 4.7 $\Omega$ is used on the transistor for high $dI/dt$, the transistor enters a cyclic turn-off oscillation, as reflected on the voltage of the free-wheeling SiC SBD. This oscillation continues for as long as the gate voltage is above the threshold on the transistor. It can be seen that the severity of peaks in SiC cascode device is lower as the rate of oscillations in this device is smaller as indicated previously. When the $R_G$ is increased to 100 $\Omega$, the $dI/dt$ in the device is reduced, and the cyclic switchings terminate.

Fig. 3. The short-circuit failure of the gate by the voltage induced by $dI/dt$ on source inductance, which discharges the DC link.

Fig. 4. The gate voltage & turn-off current measured in the drain-source of the switching transistor indicates that the spontaneous turn-on and turn-off cycles are more severe in GaN cascode, followed by the SiC cascode & standalone SiC MOSFET.

Fig. 5. Measurements are repeated with a SiC Schottky SBD with high $dI/dt$ and minimal reverse recovery charge. Self-turn-off (as oppose to crosstalk as self-turn-on) is seen in SiC SBD voltage.

Fig.6 shows the current measured in the drain-source of the transistors for gate resistances of 4.7 $\Omega$, 100 $\Omega$ & 1000 $\Omega$. It is shown that in SiC MOSFET, given the level of switching current and voltage, no unwanted turn-on or turn-off takes place. On the contrary, it can be seen that in both SiC & GaN cascodes, at 4.7 $\Omega$ unwanted turn-off takes place while at 1000 $\Omega$ unwanted turn-on initiates. This is while the switching in both cases at gate resistance of 100 $\Omega$ is not oscillatory. The values indicated although are too high for practical applications, but they demonstrate that there is an optimum switching gate resistance where unwanted positive or negative crosstalk could be avoided. Further measurements have indicated that the range of available gate resistances for the SiC MOSFET is wider than cascode devices. With SiC Cascades, as the internal capacitors are smaller than the high-voltage SiC MOSFET, there are some degree of oscillations, but these are damped promptly. The same happens with the GaN cascode device, however due to the significantly smaller size of capacitors, the continuous cycles continue until the free-wheeling current is damped in the inductor.
3. Modelling and Analysis

Cascode device packages have a range of parasitic inductances, most importantly the source inductance, that coupled with the high \( \frac{dI}{dt} \) can induce the necessary voltage to turn-off the device. These devices do not currently have the Kelvin contact which reduces the source inductance in the gate loop. Both unwanted turn-on and turn-off are heavily dependent on the switching rates. To investigate the impact of the common source inductor on the gate voltage in cyclic transients, the schematic of the circuit is modelled in LTSpice as shown in Fig. 7. The simulation models are created for all devices to analyse their switching performance theoretically. The device spice models are obtained from the manufacturers. Most values are embedded in the supplied device model, however, those that are not are extracted from the datasheets or are dependent on circuit, i.e. the gate resistances and free-wheeling inductor.

The sequence of the events at cyclic switchings is as follows: The high rate of \( \frac{dV}{dt} \) and \( \frac{dI}{dt} \) in cascode transistors causes voltage across the stray inductance and therefore, this inductor behaves like reverse biased voltage source of the gate loop and discharges the input capacitances that are being charged at the instant of turn-on phase. When the capacitors are discharged, the gate voltage of the device decreases to below the threshold voltage leading the device to turn itself off again. Once it is turned-off, the induced voltage is removed while the applied gate voltage still exists, leading to another turn-on transient with high \( \frac{dI}{dt} \) and this cycle continues.

The equivalent circuit of the common source inductor is shown as a voltage source in Fig. 7. The gate loop can be simplified and becomes a LC resonant circuit with gate-source current (\( i_{gs} \)). Eq. (1) shows the source inductance voltage as:

\[
V_S = L_s \cdot \frac{dI}{dt}
\]  

When the initial voltage of the capacitors reached \( V_{gs0} = V_{th} \), the device is turned-on. Thus, at the beginning of the transient, the gate current through the gate inductance (\( L_g \)) is approximated by \( i_{g0} = \frac{V_{th}}{R_g} \). Assuming a constant voltage on the stray inductance \( V_s \), we have:

\[
V_S = V_{gs} + R_g \cdot C_{eq} \cdot \frac{d^2V_{gs}}{dt^2} + L_g C_{eq}
\]  

In which the equivalent capacitance of the circuit device on the gate-source terminal is:

\[
C_{eq} = \frac{C_{gd} + C_{ds}}{C_{gd} + C_{ds} + C_{gs}}
\]  

With applying the Laplace transform, (2) can be written as:

\[
V_S = V_{gs}(1 + sR_g + C_{eq} + s^2L_gC_{eq})
\]  

The impact of the gate voltage can then be calculated by:

\[
V_{gs} = \frac{V_S}{1 + sR_g + C_{eq} + s^2L_gC_{eq}}
\]  

Solving the equations provides a clear understanding of the self-transients of the device. Larger gate resistance lead to lower \( \frac{dI}{dt} \), slower discharge of the input capacitances. Theoretical & simulation-based models are developed with some results of the SPICE model shown in Fig. 8. It can be seen that in both cascode...
devices, at the instant of the transistor turn-on, the free-wheeling diode turns-off in a snappy mechanism. At low gate resistances where the rate of rise of the current is too high, the turn-on mechanism of the transistor is incomplete as a negative voltage is induced on the gate, countering the positive voltage applied via the gate driver. This forces the transistor into a cyclic loop of oscillations, and it will continue until the applied gate voltage by driver is removed.

Fig. 9 is zooming on the turn-on transient part of figure 8. We can see that the cyclic oscillations are well replicated for both the GaN and SiC cascode devices. The gate voltage is oscillating which results in the oscillations of the current into the free-wheeling diode. Fig.10 shows the comparison between the measurements and models for the GaN cascode while Fig.11 shows the same comparison for the SiC cascode device.

Fig. 11. The comparison between the model and measurements of the induced gate voltage on SiC cascade transistor and the reverse recovery current of FWD at cyclic switching transients.

4. Conclusion

In this paper, the unwanted spontaneous turn-off switching of GaN and SiC cascode power devices are studied thoroughly with a wide range of experimental measurements and modelling. It is seen that both self-turn-on and self-turn-off of devices are severe in cascode transistors due to the extremely fast switching rates. Both events can lead to failure and self-turn-off at instant of turn-on transient can lead to cyclic switchings. It is shown that there is an optimum switching rate that this can be avoided.

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References