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THE IMPACT OF ELECTROTHERMAL STRESS ON THRESHOLD VOLTAGE DRIFT OF GAN AND SIC CASCODE DEVICES

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Abstract

Gallium Nitride (GaN) and Silicon Carbide (SiC) power cascode devices both take advantage of a low-voltage enhancement-mode Silicon power MOSFET coupled with a high-voltage depletion-mode GaN HEMT or SiC JFET to realize high switching frequencies with the intention of avoiding charge trapping and threshold voltage drift in the gate oxide traps of enhancement-mode SiC MOSFETs. Nevertheless, in this paper it is shown that SiC and GaN Cascodes will also suffer from the gate threshold voltage drift when subjected to significant electrothermal stress. This is partly due to the natural drift of threshold voltage in the gate, and partly due to the impact of the leakage current by the high-voltage device. The threshold voltage drift can lead to permanent degradations and potential failures, and as such is the subject of this investigation.

1. Introduction

The performance of the Gallium Nitride high electron mobility transistors (HEMT) [1, 2] which are now a competitor is some applications against SiC MOSFETs [3, 4] has been affected by the trap condition in the heterointerface. It is counted on that the donor on the surface has a great impact on the formation of two-dimensional electron gas layer (2DEG) without any deliberated external doping. Moreover, various of the traps have drawbacks in GaN HEMT structure such as kink effect, drain and gate lags [5, 6, 7]. Considering the reliability of the power devices, the stability of the threshold voltage is key matter, therefore, it is significantly important to understanding which sort of trap is responsible for the shift in threshold voltage to characterize [8, 9]. The threshold voltage of the GaN HEMTs is relied on the structure of the Al compound epitaxial layer, doping density and the AlGaN layer. Characterization of the threshold voltage during the fabrication of the device can contribute resilience in the fabrication of the devices and their applications [10]. The reliability of the SiC devices continue to be a significant issue. The surface defect of the gate oxide, and bias temperature instability has been under peculiar observation for SiC MOSFETs. The stress level on the gate can cause defects inside the insulator layer of SiO2 in the gate. These defects located on the surface or inside of the SiO2 the layer, can cause the drift of the threshold voltage [11]. The threshold voltage drift resulting from the electrothermal stress on the gate has been investigated and known caused by the positive trapped charges in the oxide layer and the interface layer, the drift of threshold voltage might be positive or negative. As the N channel MOSFETs have a negative threshold voltage shift because of the generation of the positive charges in the oxide traps, however if the interface traps have been created significantly during the bias of the stress, this may convert the direction of the shift. The change of the direction of threshold voltage drift is called the ‘turnaround effect’ [12].

In this study, the charge trapping process and threshold voltage drift of the commercially available GaN & SiC cascodes will be investigated in the off state of the devices. The threshold voltage drift in those devices under different temperatures with an aluminium hotplate has been examined and the impact of stress level on the threshold voltage drift is observed by adjusting the duration of the stress pulses and the value of the biased voltage to the gate.

2. Methodology

Commercialized devices under test are the 650 V GaN (TPH3212PS) and 650 V SiC (UJ3C065080T3S) cascodes together with the 900 V GaN (TP90H180PS) and 1200 V SiC (UJ3C120150K3S) cascodes. A fresh device is examined prior to pulsed and extended gate
stress states. To analyse the impact, pulsed and extended gate voltages have been applied with Keysight B2902A Precision Source/Measure Unit. The threshold voltage of the device is examined under various temperature from 25°C to 175°C for all cascode devices. The impact of the duration of the pulsed gate stress on the threshold voltage is observed where the stress level is from 15 to 35 V in steps of 10 V and $V_{DS} = 0.5$ V as demonstrated in Fig. 1. The duration of the stress pulses is increased from 1 ms to 1000 sec. After each pulse, 0.5 V drain voltage is biased during the sweeping of the gate source voltage from 0 V to 10 V, also the gate source voltage and the drain current are measured to observe the impact. Following, the device is recovered for 15 minutes before starting the increased stress level with 15 V, 25 V and 35 V to see the effect of each stress level on the device. The temperature impact on the threshold voltage shift by stressing of the devices is also investigated.

The schematic of the test circuits during the stress where the gate is biased with calibrated voltage and the relaxation where all terminals of the device is grounded are illustrated in Fig. 2.

The threshold voltage drift of commercially available GaN and SiC cascode devices at highest rating voltages under different temperatures are shown in Fig. 3. When the temperature increases from 25°C to 175°C, the threshold voltage decreases of 1.5 V and 0.5 V for SiC and GaN cascode devices, respectively at 650 V rating and 900 V rating.

![Fig. 1. The duration of the applied stress to the gate and drain voltage during the sweep of the gate voltage to measure threshold voltage.](image1)

![Fig. 2. The schematic of the test circuit during the gate is (a) stressed and (b) relaxed.](image2)

![Fig. 3. The threshold voltage drift of SiC and GaN cascode power device at (a) 650 V rating and (b) the highest commercially available voltage ratings, showing a decrease with temperature in all devices.](image3)

![Fig. 4. The drain current against to gate source voltage of the (a) 650 V GaN and (b) 650 V SiC cascode devices under various stress levels after the stress duration of 1000 sec.](image4)

### 3. Results

The threshold voltage drift of commercially available GaN and SiC cascode devices at highest rating voltages under different temperatures are shown in Fig. 3. When
Fig. 4 illustrates that typical drain current and gate source voltage graph for the 650 V GaN and SiC cascode power devices after each 1000 sec duration of different stress levels to the gate. As it is demonstrated on the figure, the shift in the gate source voltage has been widened by the increasing the value of the voltage to the gate with the 35 V after 1000 sec for both 650 V GaN and SiC cascode devices. This shift is much larger for the GaN than SiC cascode device. Furthermore, the reduction of the threshold voltage can cause parasitic turn-on easier with oscillations during the switching in real power applications. Regarding the stress time pulses, the drain current and gate source voltage after the 35 V stress to the gate which has a clear difference from 15 V and 25 V stress level on the 650 V GaN and SiC cascode devices. As illustrated in Fig. 5, when the stress period is longer than 100 sec, the threshold voltage is decreasing with increasing with that. As it is seen in the zoomed views of the graphs in Fig. 6, the shift of the threshold voltage has a great change under 35 V stress level and threshold voltage drift for 650 V GaN cascode device is almost 0.7 V after 1000 sec period of stress to the gate at 5 mA drain current, while this drift is nearly 0.3 V for 650 V SiC cascode device. In GaN cascode device, the turnaround effect in threshold voltage is more dominant than SiC cascode device.

Considering three different stress levels, their impacts on the drift after each stress pulses are shown in Fig. 7. It is clearly seen that there is an only large shift after 100 sec pulse of 35 V stress for the 650 V GaN cascode device, whereas it is started after 1 sec pulse of stress for the SiC cascode device. The threshold voltage shift happens clearly later in the GaN cascode than the SiC cascode device since this can be related to faster recovery of threshold voltage shift in GaN cascode device when the device turned off with grounding all terminals, there is small delay before sweeping gate voltage to measure the drain current and gate voltage.

The typical drain current and gate source voltage graphs after each set of stress levels are illustrated in Fig. 8. The changes of the gate source voltage under different stress levels are not as large as lower voltage rating of the GaN and SiC cascode devices even after each stress pulses the shift of the threshold voltage has similar trend compared to the low rated cascode devices. As for drain current and gate source voltage graphs for each duration of 35 V stress level, as represented in Fig. 9, they have the close trends for both devices. In Fig. 10, their close views of that to see the difference between rising stress times for 900 V GaN and 1200 V SiC cascode devices are shown. It is noticeably showing the turnaround impact in threshold voltage of devices, that might be happened due
to the trapping density in the interface has more pronounced impact than the trapping in the oxide layer.

Fig. 7. The shift of the threshold voltage at 5 mA drain current for (a) 650 V GaN and (b) 650 V SiC cascode devices.

Fig. 8. The drain current against to gate source voltage of the (a) 900 V GaN and (b) 1200 V SiC cascode devices under various stress levels after the stress duration of 1000 sec.

Fig. 9. The drain current against to gate source voltage of the (a) 900 V GaN and (b) 650 V SiC cascode devices under 35 V with various stress duration from 1 ms to 1000 sec.

Fig. 10. The zoomed view of the typical drain current against gate voltage graphs for (a) 900 V GaN and (b) 1200 V SiC cascode devices under 35 V stress level after each stress duration from 1 ms to 1000 sec.
The threshold voltage shift of these devices is demonstrated in Fig. 11. The threshold voltage drift in these devices is approximately 0.15 V and 0.2 V for GaN and SiC, respectively. The shift in the GaN obviously starts after 100 sec while it is 10 sec for the SiC device. As it is reported the charge trapping at SiC and SiO₂ gate insulator layers can cause the degradation of the device. These traps cause decreasing the mobility of the channel and the efficiency of the mobility as well as the drift in the threshold voltage due to the less free carriers in the channel [13]. Stabilization of the fixed and the oxide trapped charge density with the traps at the interface resulting in an appropriate threshold voltage in the device. Increasing the stress pulse length leads to instability in the threshold voltage.

Considering the temperature increase and the stressing the devices has different impact on the gate source voltage as it is shown in Fig. 12. Particularly, the gate source voltage of the 650 V GaN device has obvious difference after each stress periods. The threshold voltage of the cascode devices is increasing after stressing the GaN cascode device for 1000 sec with 35 V at high temperature. This might show that with the temperature the trap density at the gate oxide layer is increasing passing the density at the interface and the turnaround effect is not seen in the device characteristic when the temperature is increased. Considering the 650 V SiC cascode power device at high temperature, it has no impact on the transfer characteristics while stressing of the device even after 1000 sec as it is demonstrated. Furthermore, the drain current level of the devices are both decreasing at higher temperature, it is expected regarding the relationship between drain current and temperature in the power devices and also the impact of the temperature on the mobility of the devices [14, 15].

The stress duration is seen to have higher impact on the lower rated cascode devices. Since the duration of the stress is increased, the threshold voltage drift is also notably increased which is mainly related to already existing oxide traps. While the stress level is as high as 35 V, it can cause a critical irreversible shift in threshold voltage due to the trapping of the electron in the existing oxide voids and this level might generate further defects on the interface in the channel of the GaN. Under excessive stress, the high level of drift in the threshold voltage can cause the degradation of the device with decreasing the efficiency and eventual failure.
has almost no impact on the threshold voltage shift of the devices in comparison with the GaN device. In addition, temperature normally decreases the threshold voltage of the power devices [16, 17], however it is also increased by the mobility of the carriers in device structure. Therefore, it can be stated that GaN device has more pronounced increase in the mobility of the electrons in the junction and increases the threshold voltage.

4. Conclusion

This paper shows the impact of stress periods and magnitudes on the gate threshold voltages of cascode devices before sweeping. The threshold drifts after each stress lengths are illustrated. The highest level of drift is seen in the 650 V GaN cascode device in comparison with other devices. The 900 V GaN and 1200 V SiC have minor drift in threshold voltage even with longer periods of stress whereas low voltage cascode are more sensitive. With gradual increase of temperature, the GaN cascode has a clear drift in threshold voltage while the SiC cascode exhibits a temperature invariant performance.

5. References


