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Intrinsic Reliability Assessment of 650V Rated AlGaN/GaN Based Power Devices : An Industry Perspective

P. Moens, A. Banerjee, A. Constant, P. Coppens, M. Caesar, Z. Li, S. Vandeweghe, F. Declercq, B. Padmanabhan[a], W. Jeon[a], J. Guo[b], A. Salih[a] and M. Tack
ON Semiconductor, Oudenaarde, Belgium
[a]ON Semiconductor, Phoenix, AZ, USA
[b]ON Semiconductor, Gresham, OR, USA

M. Meneghini, S. Dalcanale, A. Tajalli, G. Meneghesso and E. Zanoni
University of Padova, Italy

M. J. Uren, I. Chatterjee, S. Karboyan and M. Kuball
University of Bristol, UK

Although astounding performance is already proven by many research papers, the widespread adoption of GaN power devices in the market is still hampered by (1) yield and reproducibility ; (2) cost ; (3) reliability. All three factors are to be considered, but to convince customers to adopt GaN power devices, proven device and product reliability is a must. Cost is kept acceptably low by growing the GaN epi stack on 6 inch and 8inch Si substrates, and by processing the GaN power device technology in standard CMOS production lines.

This paper will focus on the most important intrinsic reliability mechanisms for GaN power devices. It will cover gate dielectric reliability, Ohmic contact reliability, accelerated drain stress testing (high temperature reverse bias--HTRB) and high voltage device wear-out testing (high voltage off-state stress--HVOS). Acceleration models are discussed

A measurement strategy to extract valuable information about the physical properties of the buffer layers (e.g. activation energies of the traps, conduction mechanisms, …) based on simple transmission line structures, is outlined.

Introduction

Next generation high–efficient power converters require power devices capable of operating at high switching frequencies (>500 kHz) and high reverse blocking voltage (>600V). Typical applications are buck and boost converters in a PFC topology (1,2). Fast switching without sacrificing power losses allows shrinking the overall system by over a factor 4, reducing the total bill-of-materials (3).

The AlGaN/GaN material system offers a unique combination of a wide bandgap material (hence high blocking voltage capability) with the presence of a low resistive 2-dimensional electron gas (2DEG, thus low on-state resistance). Device performance is proven to be well beyond the limit of any Si power device (4,5).

Over the past years, sufficient progress was made in developing high quality MOCVD AlGaN/GaN layers with thick buffer stacks (to support >600V operation) on large Si wafers—6 inch and 8 inch. Combined with an Au-free process flow, this allows

manufacturing of GaN-based power devices in standard CMOS lines, bringing down the cost, with projected Ron*$ figure-of-merit at par or even below Si super-junction devices.

A remaining key concern inhibiting the widespread adoption of GaN power devices in the market is their unknown reliability, especially during long-term off-state stress at high temperature (HTRB), under which the 2DEG is depleted and the GaN stack behaves as a dielectric, with the threading dislocations serving as leakage paths. Voltage acceleration between 100V and 130V under HTRB condition has been observed for 100V GaN-on-Si devices (6). The importance of the buffer epi stack for off-state stress of 600V GaN-on-Si devices is discussed in (7), but without re-porting any voltage acceleration data or model. In (8), the role of space charge limited (SCL) buffer current in the dyn Ron and degradation under HTRB stress is discussed. However, no voltage-accelerated degradation under HTRB stress between 420V and 850V is observed, which is explained by the GaN buffer stack becoming resistive above a certain critical voltage (trap filling level V_{TFL}), allowing the trapped charge to leak away.

This paper will focus on the most important intrinsic reliability mechanisms for GaN power devices i.e. gate dielectric reliability, Ohmic contact reliability, accelerated drain stress testing (high temperature reverse bias--HTRB) and high voltage device wear-out testing (high voltage off-state stress--HVOS). A measurement strategy to extract valuable information about the physical properties of the buffer layers (e.g. activation energies of the traps, conduction mechanisms, …) based on simple transmission line structures, is outlined.

Devices

Devices are processed on 6 inch GaN-on-Si wafers, using a standard CMOS production line. A dedicated contamination control protocol has been established to allow mixed processing. Ohmic contacts are made using a Ti/Al based metal stack. Isolation is performed using N-implantation. Typical contact resistance Rc is around 0.8 Ohm.mm. Rhosheet of the 2DEG as measured from TLM and Van Der Pauw structures is ~420 Ohm/sq. Hall mobility and 2DEG density are ~1800 $cm^2/V.s$ and ~$9x10^{12}$ cm_{-2} respectively. The MISHEMT gate structure consists of an in-situ SiN, with an TiN/Al/TiN gate stack. Both gate and source field plates are present. The devices are passivated using PECVD SiN and poly-imide. A schematic cross-section is shown in Fig.1a. For more details, see (9). A SEM cross-section of the GaN-on-Si buffer stack is shown in Fig. 1(b). Growing GaN-on-Si results in ~10^9 cm^{-2} threading dislocations which serve as leakage paths through the buffer stack.

The fabricated power transistors have a Ron of ~100mΩ and are rated at 20A. Gate dielectric reliability is studied on gate capacitor structures of 150µm x 150µm in size (i.e. 0.0225 mm^2) with in-situ SiN and TiN/Al gate metal. Ohmic contact reliability studies are performed on standard TLM (transmission line measurement) structures, with different spacing between the Ohmic contacts.

Results and Discussion

In this paragraph the intrinsic reliability of the buffer, gate dielectric and Ohmic contacts is discussed.

Leakage and Charge Storage in the Buffer Structure

In order to well understand the reliability mechanisms in GaN-based power transistors, one needs to assess the leakage currents in the structure. Fig. 2 shows the vertical leakage current density through the GaN stack as a function of temperature. The J-V characteristic is typical for space-charge limited current (SLC), or the conduction in a dielectric through spillover from a metal (10). V_{TFL} is the voltage at which the traps in the buffer are ionized, so the quasi- Fermi level is de-pinned and moves up to the band-edge, hence the steep increase in current with voltage ($J \sim V^n$ behavior). The traps are identified using current DLTS as C-atoms on an N-site at E_v+0.85eV (8,9). Above V_{TFL}, the vertical field becomes large enough to stimulate field-enhanced Poole-Frenkel current conduction (9,11) which allows the charge in the C_N acceptors to leak away. As a result, the GaN buffer becomes resistive instead of capacitive.

Experimental support is found by doing substrate ramp experiments, see Fig. 3. By performing a negative voltage ramp on the Si substrate, the 2DEG conductivity decreases through capacitive coupling with some charge redistribution within the GaN:C layer (region "1" in the substrate ramp). The slope of the curve can be calculated from the thicknesses and dielectric constants of the different layers in the buffer structure. As from ~-300V, the undoped layer under the 2DEG starts to conducts through band-to-band tunneling. Electrons tunnel to the 2DEG, or alternatively, holes tunnel to the GaN channel region and drift to the GaN UID/SRL (strain relief layer) interface, where they are trapped because of the bandgap off-set. These holes build up the electric field across the SRL resulting in a constant field at the 2DEG for larger negative substrate bias. Hence the conductivity remains unaltered (region "2"). Finally, the complete buffer structure starts to leak and behaves as a resistor (region "3"). Upon the reverse sweep, the fixed positive charge of the trapped holes will forward bias the 2DEG to GaN channel, causing injection of electrons to neutralize the holes (region "4").

Fig. 4 shows the evolution of on-state current I_{DS} after a trap filling pulse of 1000s, as a function of recovery time and trap filling voltage. The minimum in current at around 100-200V is associated with balancing positive and negative buffer charge storage (11), but above V_{ds}=450V, almost no static IDS degradation is observed. To study the de-trapping kinetics, current DLTS at V_{ds}=200V and V_{ds}=500V is performed. Fig.5 shows the de-trapping Ron transients at T=100°C along with the proposed model, as well as the dynamic Ron (pulsed IV, t_{on}=20µs, t_{off}=2ms) from which the same effect is observed (dyn Ron is worst at 200V, and almost absent for V_{ds}>500V). The proposed model is that up to $V_{ds}=V_{TFL}$, charge redistribution (storage) occurs, but that for larger V_{ds} the current leaks away. The de-trapping transient from the C_N traps seen in Fig. 5 has two time constants with the same activation energy of 0.9eV (not shown), which we have assigned to two different leakage paths: lateral and vertical. This is supported by TCAD simulations, shown in Fig. 6, plotting the potential distribution in the off-state at 200V (near worst case condition as from Fig.4), and after switching to the on-state as a function of switch-on time. In the ON state there is initially a strong vertical field until 1000s after which charge has redistributed vertically and giving the first time constant. Then the

charge leaks away laterally to the source/drain giving the second time constant. This is reflected in two different time constants.

High Temperature Reverse Bias (HTRB)

The model that above V_{TFL}, no net charge is stored in the C-doped GaN layer and the devices become insensitive to the trap dynamics, has important consequences for any reliability test that relies on voltage acceleration. Both the degradation of the "dynamic" Ron (measured 4ms after releasing the stress voltage) and "static" Ron (measured 30s after releasing the stress voltage) are important. Fig.7(a) shows the degradation of dyn Ron at T=150°C, V_{ds}=520V, as a function of stress time for different gate-drain spacing L_{gd} (see Fig.1). The slight increase in dyn Ron (following a ln(t) behavior) indicates that slightly more charge is trapped following the stress. Shorter L_{gd} gives better performance (total amount of trapped charge in the access region is smaller). However, for too short L_{gd}, the degradation becomes larger due to too high lateral field, indicating the subtle balance between device design and buffer epi design. Fig. 7(b) shows the data at T=150°C, for one L_{gd}, with different stress voltages. Between 420V and 600V no voltage acceleration is observed, in line with the model that above V_{TFL} no net charge is stored in the buffer stack. Although there is some statistical spread on the data, the increase in dyn Ron is limited to a few%, and shows a saturation as a function of stress time (ln(t) behavior).

A wider voltage stress window is explored in Fig. 8, where transistors are stressed in off-state at T=150°C, from V_{ds}=100V up to 750V. For V_{ds}>300V, there is no degradation in the static Ron (<few %). The worst case condition corresponds to Vds~100V, in agreement with Fig. 4. After the initial increase in static Ron after 1s of stress (~10%), no additional degradation is occurring. The data clearly show that the devices are stable as function of stress time and voltage, hence there is no voltage acceleration on the degradation, in line with the SCL current model (Fig.2). The exception is V_{ds}=100V, which is the worst case balancing condition for positive and negative buffer charge. Hence the initial increase in Ron, which remains stable afterwards during stress.

Fig.9 shows the Ron degradation under off-state HTRB stress at V_{ds}=600V, for two different temperatures. Since to a first order V_{TFL} is independent of temperature (see Fig. 2), no impact of temperature on device degradation during HTRB is observed.

Buffer Wearout—High Voltage off-state Stress (HVOS)

Since the GaN buffer stack behaves as a (leaky) dielectric, one can apply high voltage TDDB during which the GaN buffer stack is stressed in off-state at high voltage until failure. This so-called high voltage off-state stress (HVOS) consists in applying a high voltage to the drain of the large area power device, the substrate and the source are at ground, and the gate is in pinch-off. The drain leakage current is monitored during the stress, and the devices are stressed till failure. High voltage off-state stress on high voltage power transistors is reported in (7,12). In (7), large area devices were stressed till failure at RT, at V_{ds}=700V and V_{ds}=750V. In (12), large area power transistors were stressed at T=80°C, at V_{ds}=1100V and 1150V. An inverse power law was used for field acceleration.

Here large area power transistors (Ron~100mΩ) are stressed at V_{ds}=900V, 925V and 950V. The ambient temperature was increased until 200°C to induce failure of the GaN buffer stack within a reasonable measurement time. The time-to-failure distributions at

V_{ds}=900V, 925V and 950V are plotted on a Weibull plot in Fig.10. The data seem to follow a Weibull distribution (as expected), albeit that the distribution is bimodal. This is attributed to wafer-to-wafer variation and within wafer non-uniformities in the buffer stack itself. Three common field acceleration models are used to extrapolate the data to 600V : E, 1/E and Poole-Frenkel. The E-model is the most conservative model, but based on the data of Fig.2, the Poole-Frenkel model is selected. This yields a time-to-fail of 10 days at 600V, at T=200^{o}C at the 100ppm level.

Gate Dielectric Degradation.

Gallium Nitride (GaN) based power should exhibit low gate leakage, especially at elevated ambient/operating temperatures (13,14). Standard gate design for these devices is based on MIS (Metal-Insulator-Semiconductor) architecture in order to suppress gate leakage current during on (forward gate bias) and off (reverse gate bias) state condition. MOCVD grown in-situ Silicon Nitride (SiN) has been the most ideal choice so far due to its lattice matching qualities with the (Al)GaN crystal.

First the conduction mechanisms under forward and reverse bias condition through the Metal/SiN/AlGaN gate dielectric stack have to be identified. Under forward bias, the voltage drop is completely over the SiN, hence the field can be easily estimated. Fig. 11 plots the forward bias current density in a Poole-Frenkel (PF) plot i.e. ln(J/E) versus sqrt(E). Clearly, the data follow a PF behavior, which is expected for a SiN dielectric. The fit of the PF model to the data is near-perfect. Out of the fitting, the barrier height of the trap, or trap energy level is extracted, and found to be 0.89 eV (15).

Having established the current conduction mechanisms in the SiN dielectric, one can proceed to the dielectric stressing experiments: constant field stress (TDDB). Fig. 12(a) shows the Weibull distribution at 5 different stress fields. The full lines represent the Weibull model fit, using the PF model for field acceleration. Lifetime extrapolation calculations using PF model revealed an operational voltage of ~5V for 10 years operation at T=150^{o}C for the SiN only dielectric calculated at 100ppm. Normalization of all the data to one stress field, results in Fig. 12(b). Clearly all the data are one single Weibull curve with slope β=2.35, data from different fields are nicely distributed, supporting the validity of our model and assumptions.

Forward voltage stress is also carried out at different temperatures, but little temperature acceleration is observed (15).

Ohmic Contact Reliability

Due to the high electric field and self–heating generated in the drain area, degradation of the ohmic contacts can affect device lifetime (16). Au–based contacts have proven to be a significant reliability issue at elevated temperatures in GaAs and InGaAs based HEMTs (17). In AlGaN/GaN based HEMTs, ohmic contacts with standard Au-based metallization seem to warrant sufficient stability under elevated temperature life-testing (18). Since large scale production of AlGaN/GaN HEMT devices in Silicon CMOS fabs requires Au–free processes, the stability in Au–free ohmic contacts subject to electrical stress need to be thoroughly studied and the failure mechanism inherent to the metallization scheme has to be researched. Very few reports have been published on the robustness and reliability of Au–free ohmic contacts (19).

In this paper, the reliability of Au–free Ohmic contacts under electrical and temperature stress was evaluated using Transmission Line Method (TLM) structures. In

order to have a measurable degradation in a reasonable amount of stress time (typically 10^4s), the TLM structures were stressed in saturation regime. Since the saturation current is different for each TLM spacing, the structures were stressed at constant power ($V_{stress} \times I_{stress}$ kept constant). The saturation current is monitored and the stress voltage is continuously adapted over time to maintain a constant power during stress measurement. The total resistance is extracted in the linear regime.

Fig. 13(a) shows the time evolution of the permanent total resistance degradation measured for different constant power stresses at 125°C on TLMs with 18µm spacing. The permanent resistance degradation features a fast degradation with stress time, followed by a hard saturation around 10%. The time evolution of the degradation is identical for all stress power levels, higher stress powers shift the curves to lower time. Although the saturation current is similar for the different powers, TLMs operate at higher voltage for higher power stress. This is a strong evidence for voltage and not saturation current as the dominant degradation driver during stress of TLMs with a given spacing. Also, TLMs with larger spacings just shift the degradation curve to longer stress times, but the overall shape of the curve is unaltered, as shown in Fig. 13(b).

To make a life–time prediction of the permanent resistance degradation as a function of contact spacing and stress power, time–to–failure has been extracted at 10% degradation as failure criteria for all stress conditions. The time to reach a predefined failure criterion such as a 10% permanent change in resistance is plotted in Fig. 14(a), and the data yields an estimate of the mean time–to–failure for each stress power and contact spacing. Lifetime extrapolation was based on the fitting of both exponential or power–law models to the experimental data. Both models fit the accelerated data well. However, the exponential model predicts a finite time–to–failure with zero power applied stress condition, which is unrealistic. Therefore the power law model is estimated to be closer to reality. As such it is possible to extrapolate time–to–failure toward lower power, and an operating power of 0.4 W at 125°C guarantees 10 years lifetime at the 10% level considering 18µm spacing.

The interacting effects of temperature and power during stress have been studied for 6µm spacing stressed at 1.25W under dark conditions at various temperatures. Fig. 14(b) shows the time evolution of the permanent total resistance degradation as a function of the chuck temperature ranging from 30°C to 200°C. Although all the curves saturate at ~10%, time–to–failure at which degradation occurs strongly depends on temperature, and all degradation curves are shifted along the stress time axis, the shift being determined by temperature. The slope of the degradation curves remains the same. The time to reach a predefined failure criterion such as a 10% change in resistance for different effective temperature was extrapolated. Based on Arrhenius plot, an activation energy of 1.04eV was extracted for permanent degradation, closely matching values reported in the literature 0.84 – 0.91eV for experiments performed on similar technologies.

Conclusion

The most important intrinsic reliability mechanisms of GaN-on-Si based power devices are discussed : buffer reliability under HTRB and HVOS stress ; gate dielectric reliability under TDDB stress ; Ohmic contact reliability under higher power stress. None present a show-stopper for GaN-on-Si power devices to enter the market.

References

1. Y. Uemoto et al., “GaN monolithic inverter IC using normally-off gate injection transistors with planar isolation on Si substrate,” IEDM Technical Digests, pp.165-168 (2009)
2. M. Ishida, T. Ueda, T. Tanaka and D. Ueda, “GaN-on-Si technologies for power switching applications”, IEEE Trans. Electron Devices, vol 60, (10), pp. 3053-3059 (2013).
3. W. Zhang, X. Huang, F. C. Lee and Q. Li, “Gate drive design considerations for high voltage cascode GaN HEMT”, Proc. APEC, pp. 1484-1489 (2014).
4. O. Hilt, F. Brunner, E. Cho, A. Knauer, E. Bahat-Treidel and J. Wurfl, "Normally-off high-voltage p-GaN Gate GaN HFET with carbon-doped buffer", Proc. ISPSD, pp. 239-242 (2011).
5. M. True et al., “The role of silicon, silicon carbide and gallium nitride in power electronics”, IEDM Technical Digests, pp.147-150 (2009).
6 A. Lidow et al., “Enhancement mode gallium nitride transistor reliability”, Proc. IRPS, pp. 2E11–2E15 (2015).
7 M.A. Briere, “Commercially viable GaN–based power devices”, Proc. Applied Power Electronics Conference and Exposition (APEC), (2014).
8 P. Moens et al., “Impact of buffer leakage on intrinsic reliability of 650V AlGaN/GaN HEMTs”, IEDM Technical Digests, s35p2, Washington DC, USA (2015).
9 P. Moens et al., “On the Impact of Carbon-Doping on the Dynamic Ron and Off-state Leakage Current of 650V GaN Power Devices”,.Proc. of ISPSD, p. 37-40, (2015).
10. M. Lampert, “Simplified theory of space–charge–limited currents in an insulator with traps”, Phys. Rev., Vol. 103, pp. 1648–1656, (1956).
11 M. Uren et al., “Electric Field Reduction in C-doped AlGaN/GaN on Si High Mobility Transistors”, Electron Device Letters, vol 36 (8), pp826-828 (2015).
12 T. Kikkawa et al., “Commercialization and reliability of 600 V GaN power switches”, Proc. of IRPS, pp. 6C11–6C16 (2015).
13 Y. Wu, C. –Y. Chen, J. A. del Alamo, “Activation energy of drain–current degradation in GaN HEMTs under high–power DC stress”, Microelectron. Rel., vol. 54, pp. 2668–2674 (2014).
14 J. A. del Alamo and J. Joe, “GaN HEMT reliability”, Microelectron. Rel., vol. 49, pp. 1200–1206 (2009).
15 A. Banerjee et al., “On Conduction Mechanisms through SiN/AlGaN based Gate Dielectric and Assessment of Intrinsic Reliability”, IRPS, Pasadena, CA, USA. Accepted for publication (2016).
16 G. Meneghesso, M. Meneghini, A. Tazzoli, N. Ronchi, A. Stocco, A. Chini and E. Zanoni, “Reliability issues of Gallium Nitride High Electron Mobility Transistors”, Int. J. Microwave Wireless Technology.,Vol 2, pp. 39–50 (2010).
17 G. Meneghesso, F. Magistrali, D. Sala, M. Vanzi, C. Canali, and E. Zanoni, “Failure mechanisms due to metallurgical interactions in commercially available AlGaAs/GaAs and AlGaAs/InGaAs HEMTs”, Microelectron. Rel., vol. 38, pp. 497–506 (1998).
18 Y.C. Chou, D. Leung, I. Smorchkova, M. Wojtowicz, R. Grundbacher, L. Callejo, Q. Kan, R. Lai, P.H. Liu, D. Eng, and A. Oki, “Degradation of AlGaN/GaN

HEMTs under elevated temperature lifetesting", Microelectronics Reliab., vol. 44, pp.1033–1038 (2004).

19 T. L. Wu, D. Marcon, S. Stoffels, S. You, B. De Jaeger, M. Van Hove, G. Groeseneken, and S. Decoutere, "Stability Evaluation of Au-free Ohmic contacts on AlGaN/GaN HEMTs under a Constant Current Stress", Microelectron. Rel., vol. 49, p. 1222 (2009).

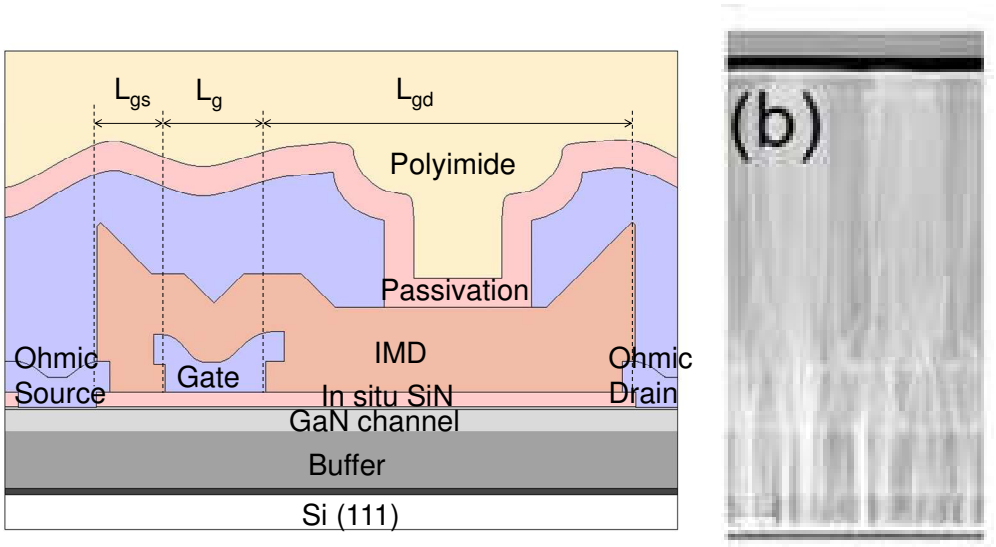

Figure 1 : (a) Schematic cross-section of the AlGaN/GaN HEMT power transistor. (b) SEM cross-section of a typical GaN stack grown on Si. Note the high density of dislocations.

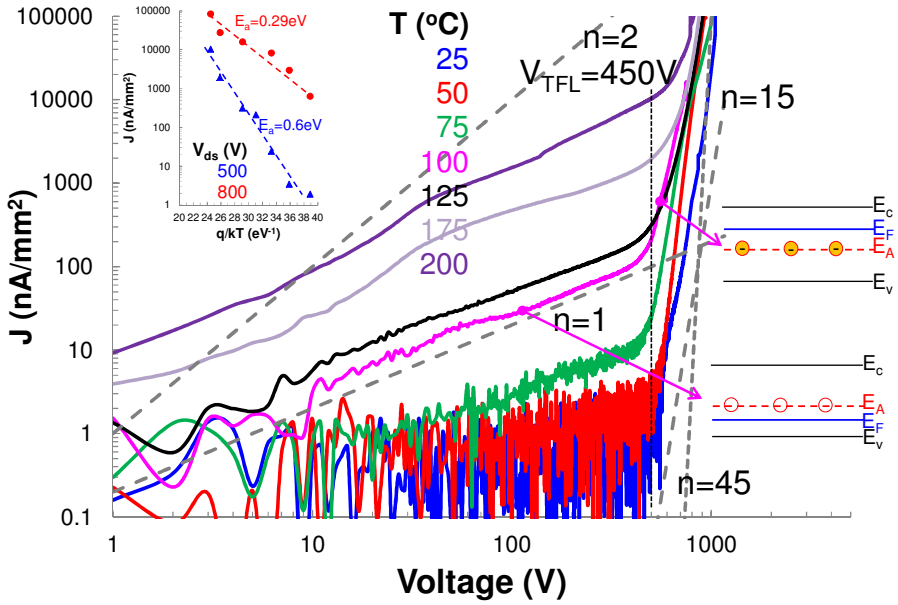

Figure 2 : ln(J)-ln(V) characteristic of the vertical leakage current as a function of temperature. The trap filling voltage V_{TFL} is the voltage at which all acceptor traps are ionized (see (10)), Note the Ohmic conduction (n=1) till $V=V_{TFL}$. Above V_{TFL}, the current through the buffer increases rapidly. Electrons are injected from the Si substrate by thermionic emission with E_a=0.6eV.

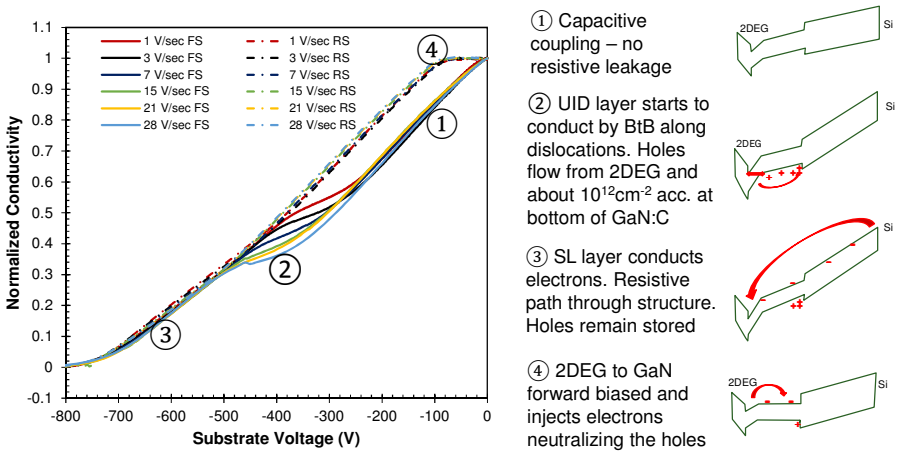

Figure 3: Substrate ramp experiment, for different ramp-rates of the back-gate voltage sweep, along with a schematic representation of the band structure of the device under the drain contact.

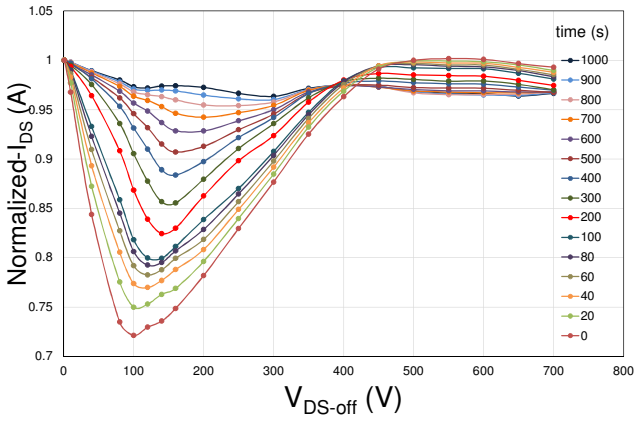

Figure 4 : Recovery of the on-state current as a function of relaxation time, after a 1000s trap filling pulsed at T=60°C, up to V_{ds}=700V. Note that from 450V, insignificant dynamic Ron is observed. This voltage corresponds to V_{TFL} from Fig. 2.

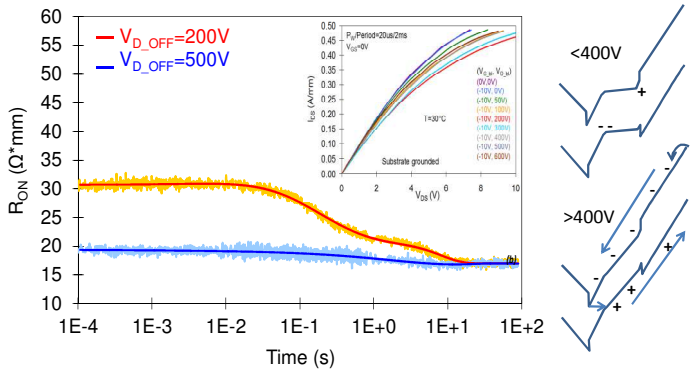

Figure. 5 : current DLTS spectra at T=100°C, after a 100s trap filling pulse at 200V and 500V. Insert : Pulsed I-V showing that dyn Ron is worst around 200V, and becomes better for higher voltage. At V=V_{TFL}, all traps are emptied and no net charge is stored any longer in the C_N traps.

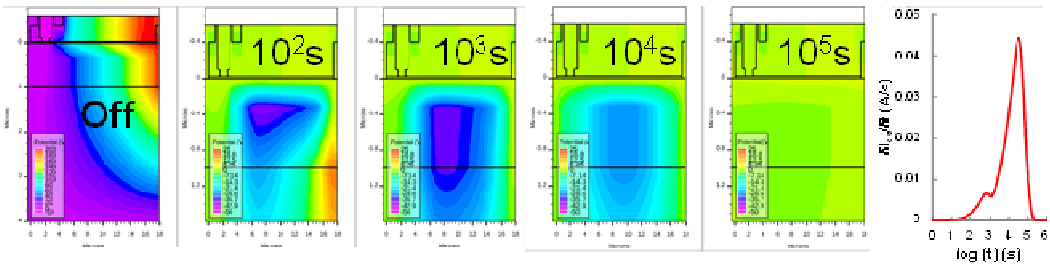

Figure 6 : Simulated potential distribution in the device, after switching from off-state to on-state, for different recovery times. Off-state condition is V_{ds}=200V, scaling of the potential is from -10V to +200V. On-state plots after 10^2s, 10^3s, 10^4s and 10^5s after switch-on ; scaling of the potential is from -50V to +25V for better readability of the plots. The last graph shows the simulated derivative of the drain current during the on-state recovery. Two distinct time constants are observed, which correlate with a vertical and lateral leakage path for the charge stored in the C_N traps, at ~10^3s and 10^4s respectively.

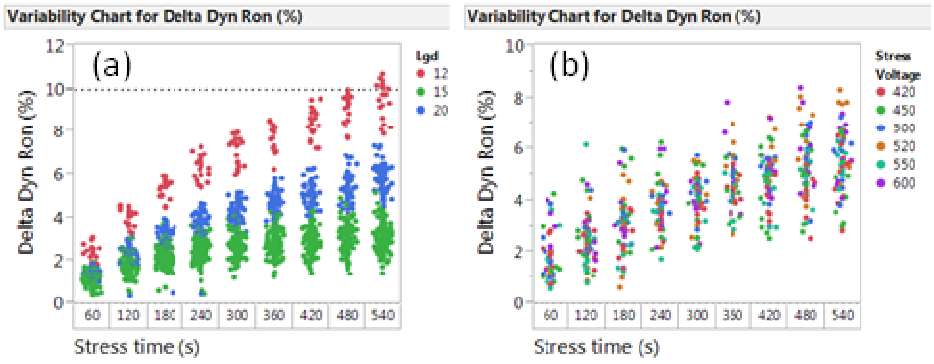

Figure 7 : Dyn Ron Measurements on 100mΩ power transistors at T=150°C. (a) dyn Ron increase measured as a function of HTRB stress time at V_{ds}=520V, for different L_{gd}. (b) dyn Ron increase as a function of HTRB stress time for L_{gd}=20µm, for stress voltages ranging from 420V to 600V. Dyn Ron is measured at the drain stress condition.

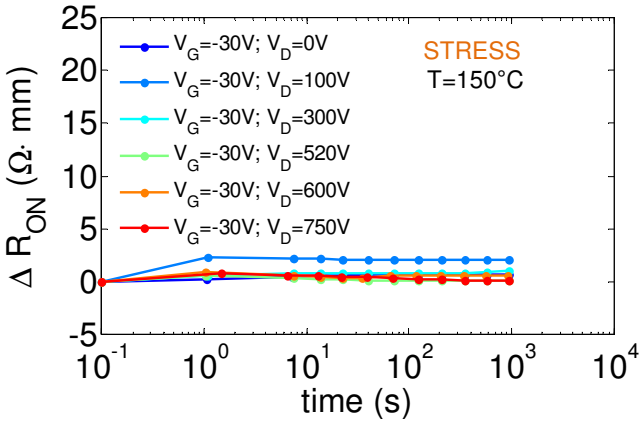

Figure 8 : HTRB stress in off-state, T=150°C, for different drain voltages. Initial Ron@150°C=20Ω.mm.

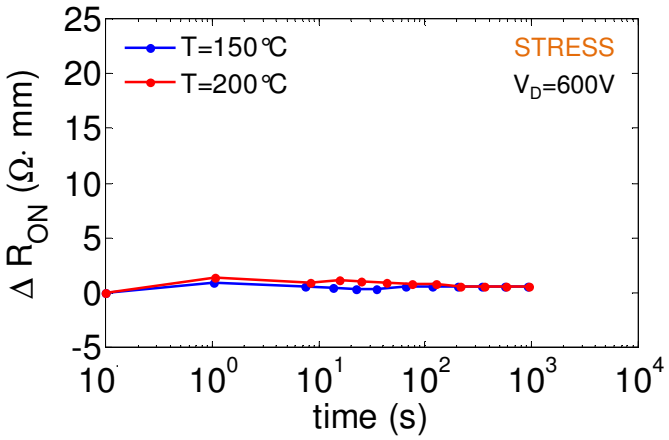

Figure 9 : HTRB stress in off-state, V_{ds}=600V, for different temperatures. Initial Ron@150°C=20Ω.mm, Initial Ron@200°C=24Ω.mm.

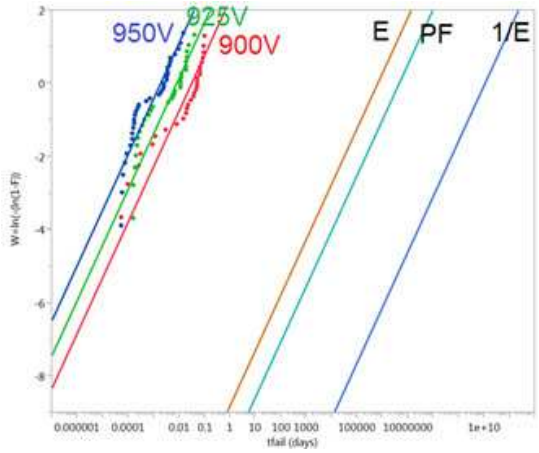

Figure 10 : High voltage off-state stress at T=200°C, on 100mΩ power transistors, at V_{ds}=900, 925 and 950V. Data are plotted on a Weibull plot, three different extrapolation models are used : E, 1/E and Poole-Frenkel. Field extrapolation for the three models is done at T=200°C, V_{ds}=600V.

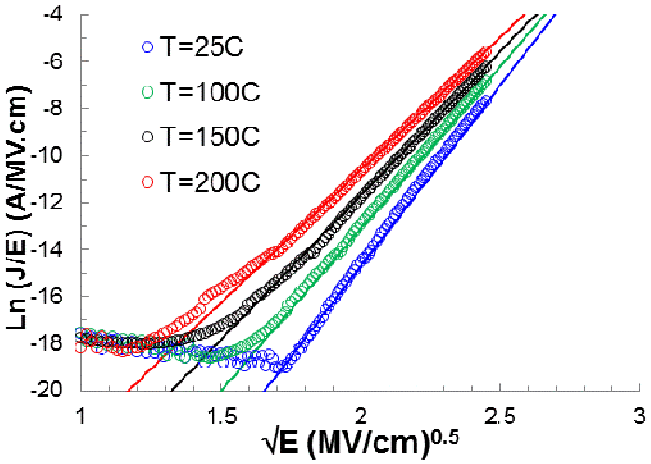

Figure 11 : Poole Frenkel (PF) plot under forward bias condition for different ambient temperatures. Symbols denote experimental data, full lines are the fit of the PF model. Data obtained on capacitor structures.

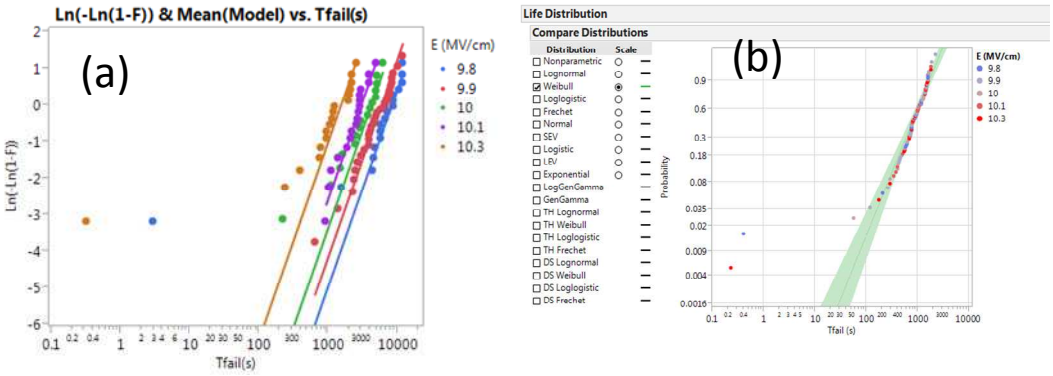

Figure 12 : (a) Weibull distribution and model fit at T=150°C, for five different gate stress fields (forward conduction). The field extrapolation model used is PF ; (b) Normalization of the TDDB data of Fig. 12 to one stress field, using the PF field acceleration model. Weibull slope β=2.35.

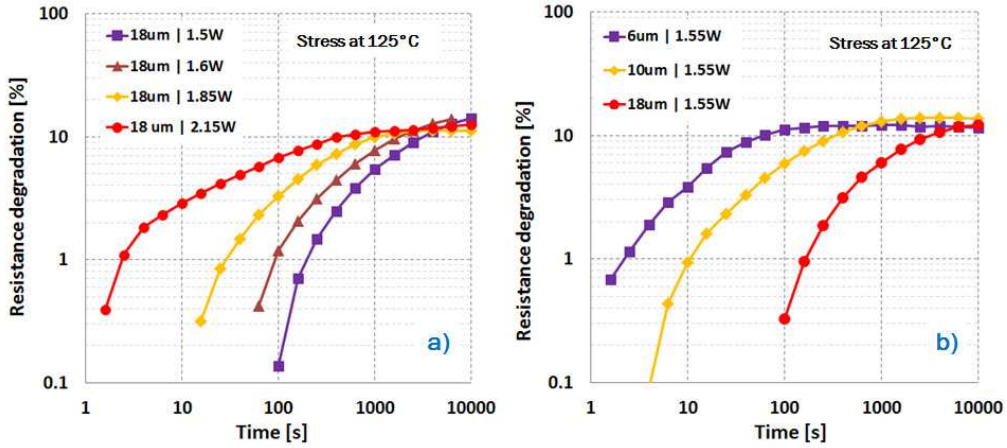

Figure 13 : Time evolution of the permanent total resistance degradation as a function of (a) constant power stress measured at 125°C on 18µm contact spacing ; (b) during 1.55W constant power stress at 125°C for 6, 10 and 18µm contact spacings.

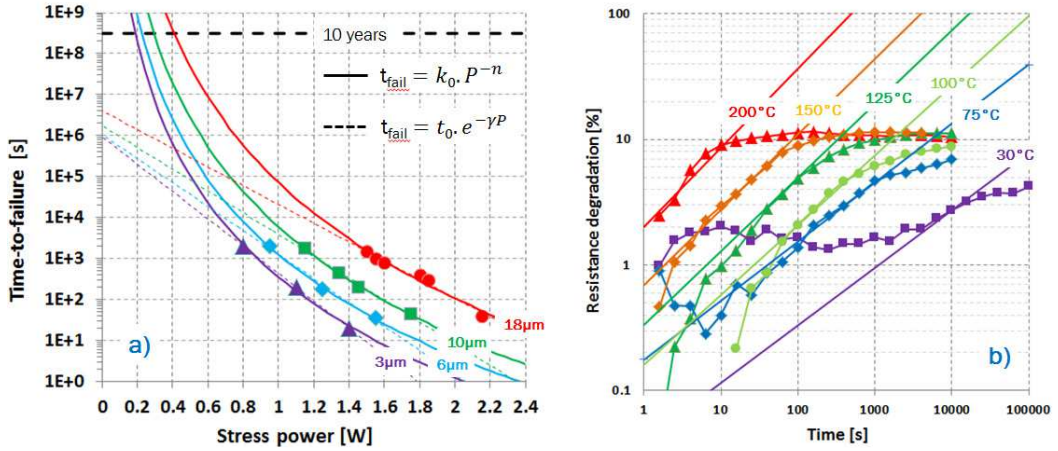

Figure 14 : (a) Evolution of time−to−failure extracted at 10% degradation as a function of constant stress power at 125°C for different contact spacing. Data are fitted by means of power law (continuous line) and of exponential law (dashed line). (b) Time evolution of the total resistance degradation as a function of chuck temperature for 6µm contact spacing stressed at a constant power of 1.25W.