"Leaky Dielectric" Model for the Suppression of Dynamic R_{ON} in Carbon Doped AlGaN/GaN HEMTs

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***Abstract*—GaN-on-Si power switching transistors that use carbon doped epitaxy are highly vulnerable to dynamic R_{ON} dispersion, leading to reduced switching efficiency. In this paper we identify the causes of this dispersion, using substrate bias ramps to isolate the leakage paths and trapping locations in the epitaxy, and simulation to identify their impact on the device characteristics. It is shown that leakage can occur both vertically and laterally and we suggest that this is associated not only with bulk transport, but also extended defects as well as hole gases at heterojunctions. For exactly the same epitaxial design it is shown using a "leaky dielectric" model that depending on the leakage paths, dynamic R_{ON} dispersion can vary between insignificant and infinite. An optimum leakage configuration is identified to minimize dispersion requiring a resistivity which increases with depth in the buffer stack. It is demonstrated that leakage through the undoped GaN channel is required over the entire gate to drain gap, and not just under the contacts, in order to fully suppress dispersion.**

***Index Terms*—Power electronics, current collapse, dynamic R_{ON}**

I. Introduction

GaN based power transistors are rapidly being commercialized for power switching applications. The excitement arises from GaN's basic materials properties of high breakdown field, good mobility, high carrier density and good thermal conductivity. These give unmatched low on-resistance with high off-state voltage, all delivered on 6" or 8" GaN-on-Si which can be processed in existing Si fabrication lines[1]. However, despite the obvious promise, take-up of the technology has taken considerable time due to technological challenges such as the naturally depletion-mode nature of the technology and difficulties in achieving insulating gate operation. Here we will concentrate on the issue of trapping in the epitaxial layers under the 2DEG. GaN on Si epitaxy has many variants but the widely employed generic structure discussed here is shown in Fig. 1a. It uses an AlGaN top barrier to create the polarization induced 2DEG, an undoped or unintentionally doped (UID) GaN channel region with the 2DEG at its upper heterojunction, a carbon doped GaN region (GaN:C) with a heterojunction at its bottom interface, a strain relief/voltage blocking layer (SRL) which may be composed of a superlattice or stepped or graded AlGaN layers, and finally an AlN nucleation layer on the Si substrate. There has been very little discussion and understanding of the function of each of these layers from an electrical standpoint; this paper will concentrate on the role of the critical upper layers at low to moderate fields.

A key issue with GaN HEMTs is current-collapse, known in the case of power devices as dynamic R_{ON} [2]. This arises due to charge trapped during off-state operation impacting on-state resistance. Trapping at the surface is now controllable by dielectric encapsulation together with a well-designed field plate[3], however trapping in the bulk of the epitaxy is an especial problem for carbon doped GaN devices. One particular issue is the extreme variation in behavior seen between different implementations using apparently the same basic layer structure[2], suggesting that this architecture has an inherent sensitivity to trapping [4]. Here we will describe a "leaky dielectric" model for the trapping and charge transport which gives a consistent explanation for this sensitivity and the enormous range of possible behaviors [5]. The model is based on the role of deep acceptors and donors as charge reservoirs, with a key difference between epitaxies being the leakage paths to those traps rather than the traps themselves. Hole transport within the GaN:C layer, and leakage to that layer, are identified as being the causative processes. Solutions to current collapse have been proposed in the past based on the model of localized hole injection to neutralize trapped electrons using either a p-GaN gate region located next to the drain [6] or a photonic-ohmic drain [7]. We show that hole injection from the drain alone is insufficient and a leakage path providing a source of holes is required over the entire gate to drain gap to fully suppress dynamic R_{ON} [8]. We show that the optimum device configuration for low dispersion is a resistivity which increases from top to bottom in the epitaxial layers. This paper primarily discusses the model, with additional experimental details available in previous papers.

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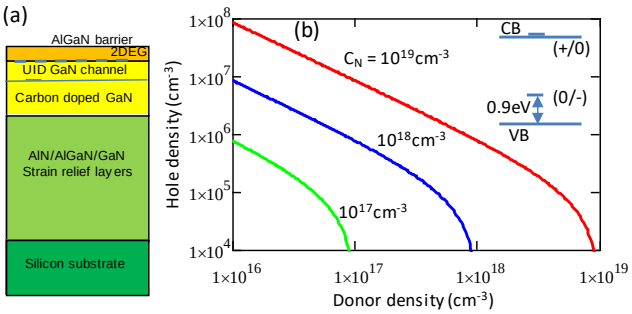

Fig. 1. (a) Generic epitaxial layer structure. (b) Free hole density as a function of compensating donor density at the indicated carbon acceptor densities. The inset shows the trap energy levels. The donor level is not critical provided it is above the acceptor level.

II. Models

This section reviews the impact of trap energy level and compensation on free carrier density, and the impact of epitaxial resistivity on charge storage.

A key part of the structure is the highly resistive GaN:C layer, however its electrical behavior has been little studied. Carbon can be incorporated during GaN growth substitutionally on either the N or Ga site, with the most recent calculations[9, 10] and spectroscopy[11] assigning C_N as a deep acceptor (ie neutral or negatively charged) 0.9eV above the valence band, and C_{Ga} as a donor (ie either neutral or positively charged) in the conduction band. Earlier papers suggested that auto-compensation would occur with exactly equal numbers of substitutional C_N and C_{Ga} [12-14]. However which site is favored is now believed to depend on kinetic factors as well as the Fermi energy at the growth temperature, with MOCVD grown material favoring the N site [10].

Based on this level assignment, the dominant C_N acceptor trap level in heavily doped GaN:C is expected to be in the lower half of the bandgap, meaning that majority carriers will be holes and the material will be p-type. If there were no donors, a typical carbon concentration of $2x10^{18}cm^{-3}$ would result in a hole density of $\sim10^{11}cm^{-3}$ and resistivity $\sim10^{6}$ohm.cm, whereas in one device the inferred GaN:C resistivity was $5x10^{13}$ohm.cm [5]. This discrepancy can be explained since in addition to C_N, there will always be donors whose density is generally unknown. Those with energy levels above the C_N level (such as C_{Ga}, oxygen or silicon impurities) will impact the C_N occupancy and increase resistivity. Fig. 1b shows how the calculated free hole density varies with donor density for C_N densities of 10^{17}, 10^{18}, $10^{19}cm^{-3}$; it demonstrates the standard semiconductor statistics result that hole density is proportional to the *ratio* of the compensating donor density to the C_N density [15, 16]. For a typical carbon doping density in the 10^{18} to $10^{19}cm^{-3}$ range, a compensation ratio between 0.1 and 0.6 is required to produce a free hole density in the C-doped GaN layer in the range $2x10^{5}$ to $10^{4}cm^{-3}$, corresponding to a resistivity of 10^{12} to 10^{14}ohm.cm for a mobility of 10-100cm^2/Vs. Hence high compensation is required for consistency with experiment [5].

When an external vertical electric field is applied to the GaN:C layer, there are two limiting cases. Firstly, under transient conditions or where non-blocking contacts are made to the material, the layer will behave resistively with the Fermi level pinned near the bulk level (Fig. 2a). Secondly if the GaN has a blocking contact such as a heterojunction or a reverse biased junction, then a depletion region can form under static conditions. For the standard field polarity of a positive bias on the transistor drain terminal the width of this depletion region will be determined by the C_N density at the top (Fig. 2b) or the compensating donor density at the bottom of the GaN:C layer (Fig. 2c). With a blocking heterojunction, a 2D hole gas can form at the bottom of the layer for sufficiently high field (Fig. 2c) [17, 18]. Under static bias where there is no significant substrate leakage, it is these regions that will store the majority of the charge which leads to current collapse.

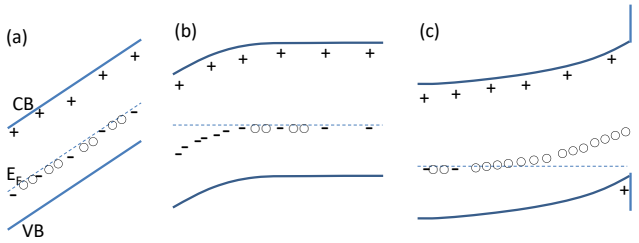

Fig. 2. Band diagrams for the GaN:C layer illustrating the effect on trap occupancy of the applied electric field with negative substrate bias. (a) Ohmic contacts to top and bottom of the layer, (b) depletion region at the top and (c) depletion region and blocking heterojunction at the bottom of the layer.

Linearizing the transport, the resistance and capacitance per unit area of this layer will be $R = \rho d$ and $C = \varepsilon/d$ where ρ is the resistivity, ε the dielectric constant and d the thickness. The time constant for self-discharge of the charge on the surfaces will be $\tau = RC = \varepsilon\rho$. The interesting point here is that the self-discharge time is thickness independent and only dependent on the resistivity. For the GaN:C layer this means that trap responses in substrate bias transient experiments or DLTS would have a minimum time constant in the range 1-100s for the compensation ratios discussed earlier. Typically, carbon doped transistors show transient time constants in the 1-1000 seconds range[19] consistent with the resistivity discussed earlier.

The epitaxy can be treated as a leaky dielectric stack, where charges will accumulate at interfaces between layers of different resistivity as a result of the Maxwell-Wagner effect[20]. If we apply the standard field polarity across this layer, it will result in a static positive charge $Q = CIR = \varepsilon\rho I$ at the top and an equal negative charge at the bottom, where I is the vertical current density. Applying a voltage across two stacked layers gives a charge at the interface between those layers of

$$Q_2 - Q_1 = (\varepsilon_2\rho_2 - \varepsilon_1\rho_1)I$$

where the indices 1,2 refer to layers above and below the interface respectively. Since dielectric constant changes are small in this system, charging at an internal interface will only be suppressed if the *resistivity* is constant throughout, and negative charge will accumulate if the resistivity is higher above than below any interface. Generalizing this to a multilayer stack such as the epitaxy used for GaN power

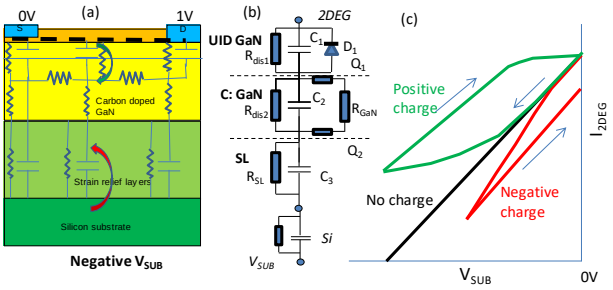

Fig 3, (a) Substrate bias ramp measurement configuration. (b) 1D lumped element representation. (c) Schematic ramp curves. Green shows leakage through the UID-GaN and red through the SRL.

transistors, we can make a general statement that suppression of bulk negative charge storage is achieved by ensuring that the resistivity increases from top to bottom in the structure.

III. Substrate Bias

A. *Vertical Transport*

In order to assess epitaxial transport and trapping, various approaches have been used including DLTS [21], and Thermally Stimulated Current [22]. Here we will concentrate on slow substrate bias ramps [5, 23], which have a response time appropriate for GaN:C, and which deliver a relatively simple "fingerprint" approach to establishing the leakage paths which are dominant.

Fig 3a shows how a substrate bias ramp experiment is undertaken. The conductivity of the 2DEG is measured using a small bias of <1V between two Ohmic contacts while the Si substrate is used as a back gate and ramped at a constant rate in a bidirectional sweep. The resulting 2DEG conductivity curve is sensing the electric field just below the channel as a function of substrate bias. Interpreting the behavior requires an equivalent circuit representation of the entire stack. The simplest assumption is that there is no lateral current flow in the stack and the 1D model of Fig. 3b applies.

Fig. 3c shows schematically the three basic behaviors which is observed for epitaxy from different sources [24] for negative Si substrate bias. The simplest case is that the entire structure behaves as an insulator and so the only active components are the capacitors. This results in a roughly constant back gate transconductance and no hysteresis (assuming constant mobility). The extrapolated back-gate threshold voltage will be $V_{TB} = -q\, n_{2DEG}/C_{TOT}$ where C_{TOT} is the series combination of C_1, C_2 and C_3. In practice, most epitaxies display a region at low back-bias where capacitive coupling dominates before significant conduction occurs in any layer. Capacitive coupling will be observed provided the leakage in all layers is less than the displacement current ie $I_{DISS} = C_{TOT}\, dV_{SUB}/dt$. If any layer starts to conduct then charge storage at nodes within the structure will occur, either as free carriers at blocking interfaces or in depletion layers resulting in a deviation from the capacitive behavior as shown in Fig. 3a,c.

Fig. 4a shows a substrate ramp experiment for a high quality layer structure measured at ramp rates of 1 and 28 V/s corresponding to displacement currents of ~2 and ~60nA/cm^2

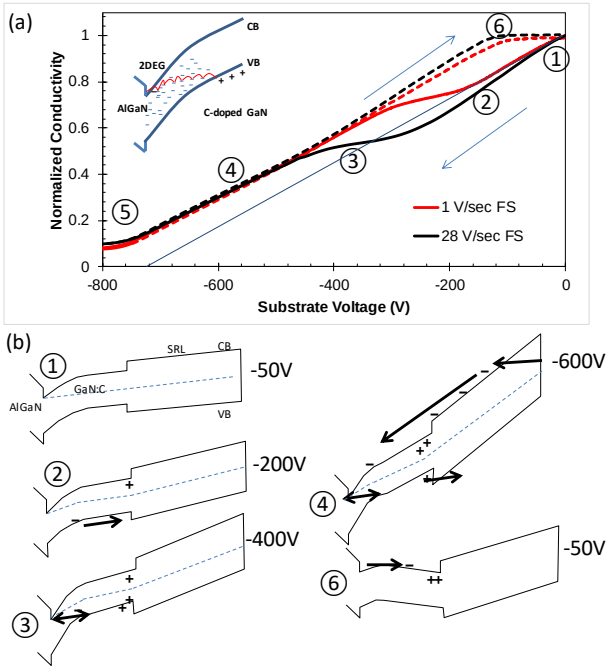

Fig 4. (a) Substrate ramp for 2 different ramp rates. Data from [25,26]. The thin line with pinch-off at -730V indicates the expected result for insulating epitaxy. (b) schematic band diagrams showing inferred charge storage locations and current flows.

[25, 26]. Fig. 4b gives schematic band diagrams showing where charge storage and leakage has been inferred for regions identified in Fig 4a. In region 1, up to about |-50|V, capacitive coupling is observed where the structure can be considered an insulator. In region 2 above |−50|V, the leakage current in the GaN:C exceeds the displacement current resulting in the small increase in transconductance observed. In this region charge redistribution only within the GaN:C layer occurs from top to bottom forming a dipole. Using the leakage onset of -50V, the value for I_{DISS} and the total thickness of the structure, we can very roughly estimate the resistivity of the GaN:C layer. This gives ~10^{13}Ohm.cm consistent with the discussion in the previous section. The maximum increase in transconductance associated with this redistribution would be a factor of $(C_1C_2 + C_2C_3 + C_3C_1)/(C_2C_1 + C_2C_3)$ which in this case is ~1.1 roughly consistent with the measurement [23]. In region 3, the current saturates indicating positive charge storage which requires that the resistivity of the UID GaN layer is now lower than the GaN:C. This requires a band-to-band leakage process in the UID GaN. Leakage across a reverse biased GaN PN diode is known to occur along extended defects by a trap assisted mechanism (an example trap-assisted mechanism is shown in the inset to Fig 4a.)[27]. The result of the band-to-band process is that an electron flows into the 2DEG releasing a free hole in the valence band. Holes flowing in the GaN:C layer will accumulate at the heterojunction at the bottom of the layer, either neutralizing acceptors and so exposing donor charge, or as free holes. This charge will reduce the UID GaN electric field resulting in the saturation observed. Region 3 extends over about 100V in substrate bias which corresponds to a positive charge of about 10^{12}cm^{-2} if located at the top of the stack.

As the field increases further into region 4, we enter the

regime where leakage starts to occur through the entire stack and exceeds I_{DISS} in all layers [25]. Further hole trapping does not occur and electron injection from the Si can start. Once the leakage exceeds the displacement current, the resistive elements in the network of Fig. 3b dominate. In region 5 at high bias, the saturation observed would be consistent with deep depletion in the Si associated with high vertical leakage, however this speculation has not been tested.

On the return sweep, the stored positive charge remains at the heterojunction and so the epitaxy behaves largely as an insulator. However once the ramp has returned to the point where the stored positive charge reverses the field under the 2DEG (region 6), this forward biases the junction between the 2DEG and GaN:C allowing electrons to rapidly flow into the GaN:C from the 2DEG neutralizing the stored positive charge [5, 28]. At the end of the ramp, the net charge in the epitaxy is close to zero and if this epitaxy were used in a transistor, there should be minimal dynamic R_{ON} as discussed later.

Further analysis of the data shown in Fig. 4 can be undertaken by extracting the turning points between regimes as a function of ramp rate and temperature. These turning points give the voltage at which conventional leakage current becomes equal to I_{DISS}. Under favorable circumstances, using the equivalent circuit of Fig. 3b allows one to extract IV characteristics for each layer in the stack [23]. In [23], the band-to-band leakage through the UID-GaN channel layer was fitted by a Poole-Frenkel model with an activation energy of about 0.6eV, but more likely it corresponds to the hopping energy for the band-to-band process[29]. Transient measurements of conduction in region 2 in [23] showed an activation energy of 0.85eV, consistent with charge redistribution in the GaN:C layer and activation of holes to the valence band from the C_N acceptor.

B. Effect of 2D and 3D transport on substrate ramp

By examining different device geometries, the substrate ramp technique can identify situations where the assumption of vertical current flow breaks down. Here we discuss two examples of where lateral current flow exists in the epitaxy, meaning that the simple 1D model of the previous section can only be used with care.

Fig. 5 shows an example similar to that discussed in [5]. Here the Ohmic contact gap used to sense the 2DEG conductivity is varied between 8 and 18µm. A strong dependence of the behavior on contact gap is observed with a trend towards capacitive behavior at large gap. It is quite clear that the devices have a higher vertical conductivity through the UID GaN layer under the contacts than in the gap between those contacts, perhaps due to spiking under the contacts. Extending the interpretation of the previous section suggests that this sample had a hole current flowing laterally in the GaN:C layer from an enhanced leakage path under the contacts. Large gaps result in capacitive behavior because the time-constant for charge flow from the contacts to the center of the gap exceeds the ramp time. Transient time constants for lateral charge flow in the GaN:C would be even longer than those discussed for vertical transport in section II. In contrast to the behavior of Fig. 5, other wafers

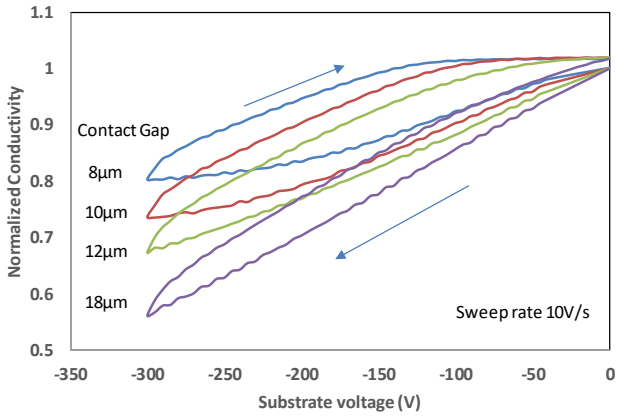

Fig. 5. Substrate ramps for a device with varying contact gap from 8 to 18µm at room temperature.

showed positive charge storage but no gap dependence indicating that leakage occurred across the entire source-drain gap [5].

Another situation which can arise, but which we will not discuss in detail here, is that charge can be observed flowing laterally outside the active device area into the implanted isolated area. This has the effect of making small and large devices show different behavior with small devices displaying large device-to-device variation [18, 30]. Our explanation for this active area size dependence is that a 2DHG is induced at the heterojunction at the bottom of the GaN:C layer by the applied electric field and heterojunction polarization charge, allowing rapid lateral flow. The inference is that the compensating donor density is too low to fully suppress the formation of such a layer as the field increases.

IV. Drain Bias Dependence of Dynamic R_{ON}

Let us now apply the observed transport in the epitaxy which we have deduced from substrate ramp measurements to the practical situation of dynamic R_{ON} in power switching transistors. Here the electric field distribution is inherently 2D, so lateral as well as vertical transport must be considered. We aim to explain the enormous variations in behavior that have been reported for carbon doped devices [2]. Punch-through under the gate can lead to lateral leakage of electrons, but it is controllable by buffer and gate design[31] and is not related to the bulk hole transport considered here.

Under off-state bias, a high positive drain bias is applied with the 2DEG pinched off under the gate and with the Si substrate acting as a ground plane. Based on the measurements described in the earlier sections, we believe that lateral and vertical hole current flow and charge accumulation can occur in the top layers in the structure. Basic electrostatics in off-state will result in accumulations of charge across the vertical and lateral capacitors shown in Fig. 6. For the vertical component of the field, a negative charge must appear in the Si under the drain (region ① in Fig.6). Matching that charge, a positive charge must occur near the top of the epitaxial layers. Exactly where that positive charge is located will depend on the relative resistivities of the GaN layers and would normally reside

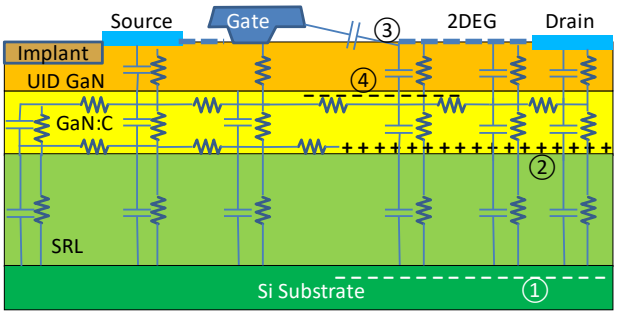

Fig. 6. Equivalent circuit representation of the power transistor showing the leakage resistance and capacitive components. The location of charged regions resulting from applied drain bias are indicated with numbers 1-4.

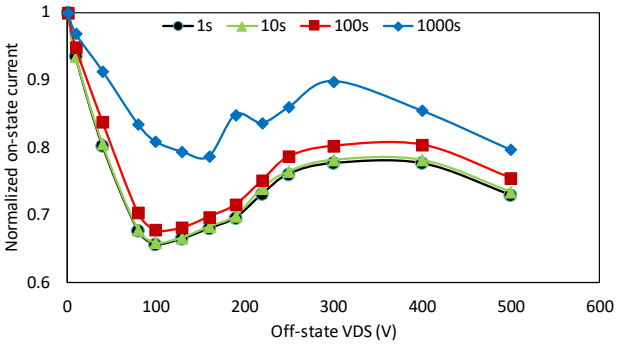

Fig. 7. Normalized on-state current for a power device measured 1, 10, 100 and 1000s after 1000s in the off-state at the indicated drain bias.

vertically anywhere between the drain contact itself and the top of the SRL. In Fig. 6 we have assumed that there is a leakage path through the UID GaN layer so the positive charge layer is located at the heterojunction (②). Any positive charge located in the epitaxy will be primarily ionized donors. This is because in contrast to the situation in a substrate ramp experiment where there is no significant lateral field, any free holes at the blocking interface at the bottom of the GaN:C will tend to be swept towards the source by that lateral field. This will prevent the build-up of a high free hole density under the drain or in the gate drain gap [6, 32].

In order to support the lateral field between the drain and gate, a positive charge must arise on the drain side of the source/gate to drain gap capacitor and a negative charge on the gate side. The positive charge will largely result from depleting the 2DEG thus exposing the positive polarization charge at the bottom of the AlGaN layer (③), and the negative charge will be shared between the gate, source field plate and ionized acceptors in the GaN (④). It is this trapped charge ④ that is responsible for the dynamic R_{ON}. All these charges must be present in all off-state biased GaN-on-Si HEMTs, however the proportion of those charges present in traps in the GaN rather than on electrodes and in the 2DEG will determine the susceptibility of the device to dynamic R_{ON}.

Fig. 7 shows a dynamic R_{ON} measurement on a power device (device shown in [30]), where it can be seen that negative charge storage reaches a maximum at an off-state drain voltage of 100V and then drops again. Note that for this device recovery following off-state stress only commences after 100s and full recovery takes thousands of seconds. A saturation and drop in dynamic R_{ON} at higher drain bias is frequently observed, see for instance [33].

In order to explore the impact of leakage paths and explain how a maximum in dynamic R_{ON} can arise, we will employ a device simulation. A generic depletion-mode Schottky gate, field plated power device has been simulated with Silvaco ATLAS using the approach described in [34]. The simulation includes Fermi-Dirac and SRH statistics but does not include impact ionization or surface traps. The epitaxial layer stack consisted of 3nm GaN cap, 20nm AlGaN barrier resulting in ~$6x10^{12}cm^{-2}$ 2DEG charge, a 0.3µm UID-GaN layer containing $10^{15}cm^{-3}$ shallow donors, a 0.7µm GaN:C layer containing $10^{19}cm^{-3}$ acceptors 0.9eV above the valence band compensated with $3x10^{18}cm^{-3}$ shallow donors, on a SRL of thickness 3µm which we represent with undoped AlN and which forms an insulating layer with blocking heterojunction to the GaN layer. The compensating donor density used in the GaN:C layer is sufficiently high to largely suppress a 2DHG until biased above 400V. Obtaining a good fit to experiment was found to require this high compensation ratio. Four different situations corresponding to different magnitudes of the leakage paths are shown in Fig. 8 [8]. The different leakage paths represent

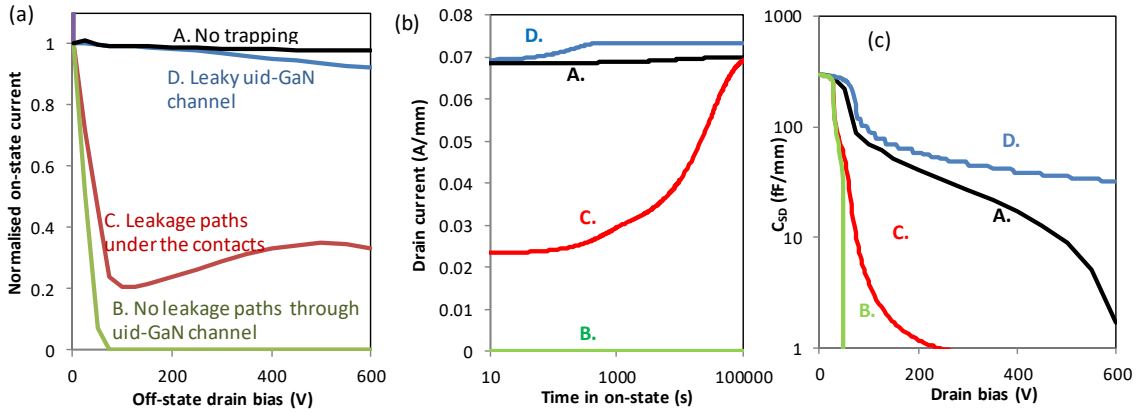

Fig. 8. Simulated response of a generic power transistor for four different limiting cases of leakage paths. (a) Drain bias dependence of the on-state conductance 1µs after switching to the on-state ie inverse of dynamic R_{ON} response. (b) Time dependence of the drain current at V_{DS}=1V, V_{GS}=0V following off-state stress at V_{DS}=400V. (c) Drain dependence of the S-D capacitance in off-state. An equilibrium off-state is used for cases B, C, and D and case A is actually case B but with only 1µs off-state time.

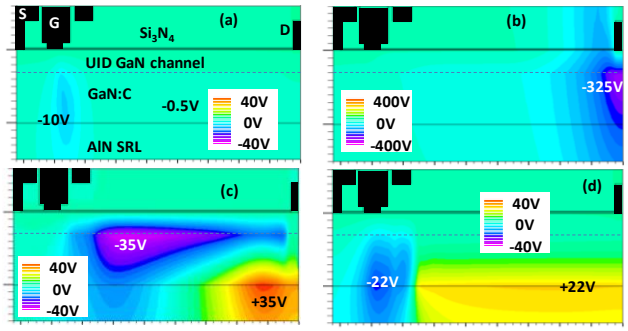

Fig. 9. Potential distribution with V_{DS}=1, V_{GS}=0V 1µs after switching from V_{DS}=400V, V_{GS}=-5V for the four simulations A-D of Fig. 8 (note different contour scale for (b)).

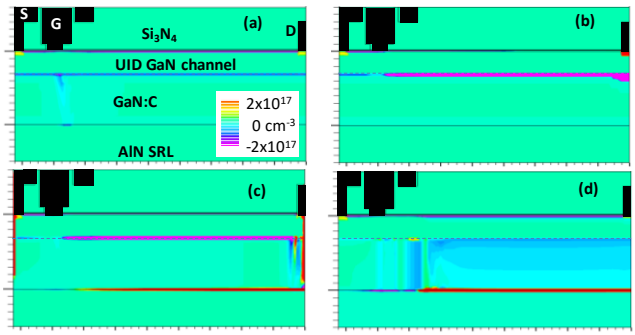

Fig. 10. Net ionized charge distribution for the simulations A-D of Figs. 8, 9 with the same conditions as Fig. 9. The scale of $\pm 2x10^{17} cm^{-3}$ has been chosen to highlight the location of the positive (red) and negative (purple) charged regions, so the maximum values exceed this range.

limiting cases and generate dramatically varying predicted dynamic R_{ON} results but without any change in the trap density or epitaxial layer structure.

(A) Insulating epitaxy where there is no charge storage, delivering minimal dynamic R_{ON}. In addition to an insulating substrate this also corresponds to the situation for short off-state times where there is insufficient time for charge to have been stored. Here the effect of a 1µs off-state time (t_{OFF}) was simulated for the model B below.

(B) A floating p-type GaN:C layer isolated from the 2DEG by a p-n junction, where there is no leakage through the UID GaN channel and where the off-state time is long enough for the potential to reach equilibrium (implemented here as t_{OFF}=infinity) [4]. This delivered infinite dynamic R_{ON} at only 40V.

(C) Leakage under the source and drain contacts to the GaN:C layer, corresponding to the situation shown in Fig. 5. This is implemented in the simulation as a heavily doped p-type short between the source and drain and the GaN:C layer, and with t_{OFF}=infinity as discussed in [5, 35]. This resulted in a maximum in dynamic R_{ON} at 100V very comparable to the experimental result of Fig. 7 [34].

(D) Leakage through the UID GaN between the 2DEG and the GaN:C layer along the entire length of the device, and which resulted in minimal dynamic R_{ON}. To achieve this result in the simulation requires that the vertical resistivity in the UID GaN is lower than the resistivity in the GaN:C. Since band-to-band leakage cannot currently be included in the simulation, this case was implemented by simply making the GaN:C n-type by adjusting the C_N trap level to be 0.9eV below the conduction band rather than 0.9eV above the valence band, hence providing an Ohmic contact between the 2DEG and the GaN:C and removing the P-N junction. (Electrically n-type GaN and p-type GaN with strong band-to-band leakage would be very comparable provided a 2DHG does not form. This situation is similar to the case of iron doping discussed in [4].)

A key concept in understanding the enormous range of predicted behavior of Fig. 8a, varying from essentially no dynamic R_{ON} to complete collapse, is that the GaN:C layer acts as a resistive back-gate with a pinch-off voltage of $V_{PGaN:C} = -qd_{UID}n_{2DEG}/\varepsilon_{GaN}$ (assuming insignificant charge storage within the UID-GaN channel layer) [34]. For the simulated device $V_{PGaN:C}$ is only −40V, so relatively small voltages associated with stored charges compared to the 600V operating voltage will have a dramatic impact on R_{ON}. Figs. 9 and 10 show the potential and ionized charge distributions in the channel region for the simulations of Fig. 8 immediately (1µs) after switching from the off-state at V_{DS}=400V to the on-state. As already discussed, there are positive and negative charged regions to support the vertical and lateral off-state fields. For (A), there is almost no epitaxial charge storage as expected. For (B), the drain bias is dropped across the UID-GaN channel under the drain so the back-gating effect pinches off the channel at V_{DS}>40V [4]. For (C), the GaN:C acts as a resistive path for hole flow between the drain and source which is decoupled from the 2DEG [34] allowing all the positive and negative regions shown schematically in Fig. 6 to form. Since the back-gate potential is locally as high as -35V, there is a significant increase in R_{ON} as seen in Fig. 8a. Interestingly the recovery of this charge with on-state time can show two time constants (visible in curve C of Fig. 8b), associated with vertical and lateral current flow within the GaN:C layer. Two time constants that are consistent with this predicted behavior have been observed experimentally [25, 26]. And for (D) the lower vertical resistivity through the UID-GaN layer results in the GaN:C staying pinned to the local 2DEG potential. This suppresses the formation of a significant negatively charged depletion region at the top of the GaN:C region, but forms a positively charged region above the heterojunction to support the substrate field, leading to almost no R_{ON} increase.

So it would appear that using either an insulating (variant A) or n-type/vertically leaky p-type GaN layer (variant D) when combined with a relatively insulating SRL would be the optimum solution to suppress dynamic R_{ON} dispersion. Achieving a truly insulating epitaxy is hard given that even GaN:C with a resistivity of 10^{14}ohm.cm is insufficiently resistive to suppress charge redistribution on a timescale of minutes for typical applied electric fields. Hence the solution suggested by these simulations in terms of full suppression of dynamic R_{ON} is to control the leakage of the UID GaN layer. The requirement for full suppression is that the resistivity of the UID GaN layer is less than or equal to the GaN:C layer over the entire desired operating bias and temperature range. This requirement is naturally achieved for n-type GaN but cannot obviously be achieved using point defects to reduce the resistivity of the PN junction present between GaN:C and the 2DEG. It seems more likely that this can be achieved by

modulating the conductivity of the 10^9 to 10^{10}cm^{-2} of threading dislocations typically present in these devices. Leakage along an extended defect through the UID GaN is highly non-linear occurring by a mechanism such as variable range hopping. Hence it is also necessary that the required leakage current through that layer must occur at applied voltages very much less than the back-gating pinch-off voltage of the GaN:C layer.

Since the GaN:C layer itself is such high resistivity, this requirement for leakage through the UID GaN layer need not lead to a significant drain leakage current, corresponding to less than 1pA/mm at room temperature for the examples given here. However, guaranteed suppression does require good control of this leakage path through a combination of epitaxial growth and processing conditions. Too good a material quality would result in strong dynamic R_{ON} and too poor a material would result in drain leakage/breakdown. The existence of device processes with very low dynamic R_{ON} based on carbon doped GaN shows that optimization of this leakage path is feasible [8]. It has recently been shown that processing can modify the UID GaN leakage. Consistent with the model presented here, changing the deposition conditions of the passivating silicon nitride layer changed the UID GaN vertical leakage, and changed the dynamic R_{ON} between insignificance and full collapse[36].

Allowing vertical conduction to occur across the entire UID GaN layer may not necessarily be the optimum solution in all circumstances. Using a GaN:C layer with shorting contacts (variant C above) allows matching positive and negative charged regions to form, resulting in a RESURF effect which reduces the lateral electric field and could increase breakdown voltage [34]. The simulated capacitances for all the leakage options are shown in Fig. 8c. The low dynamic R_{ON} dispersion options (A, D) have higher output capacitance than the case of no leakage (B) or just leakage under the contacts (C). This arises because the latter allow depletion across the entire gate-drain gap for drain bias above about 100V. In reality, an intermediate situation between the limiting cases considered here would normally occur, with UID GaN leakage occurring not only under the contacts but also across the entire gate-drain gap.

V. Conclusions

We have shown that the carrier transport in carbon doped epitaxy now commonly used for high power GaN switching transistors can be characterized and interpreted using a leaky dielectric model. Based on published substitutional carbon energy levels, the GaN:C layer is expected to be a strongly compensated p-type semiconductor of very high resistivity[10], consistent with the demonstrated importance of hole flow [6, 7]. Using the substrate ramp technique, it is found that for good quality epitaxy there is normally vertical leakage from the 2DEG down into the epitaxy resulting in positive charging of the GaN:C layer under standard drain bias conditions. This requires a band-to-band leakage path which is presumed to be largely via extended defects such as dislocations.

The leakage paths within the structure are shown to be crucial in understanding the dynamic performance of the transistor. Simulations are shown where all that is changed is the leakage path within the structure, resulting in a continuous variation between essentially no effect and infinite dynamic R_{ON}. It is shown that in the presence of a small optimized leakage path from the 2DEG down to the GaN:C layer extending over the entire gate-drain gap, the dynamic R_{ON} can be almost completely suppressed. It is clear that control of the epitaxy for GaN power transistors requires a full understanding and control of the leakage between point defects and along extended defects, as well as knowledge of the carbon density and its compensating donors.

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