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The Impact of Ti/Al Contacts on AlGaN/GaN HEMT Vertical Leakage and Breakdown

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***Abstract*— Enhanced leakage paths below Ti-/Al-based contacts to GaN-on-Si HEMTs have been identified and studied. Through a novel use of the quasi-static capacitance–voltage technique, the depth of these preferential leakage paths was determined to be ~1.6 μm, extending down into the superlattice strain relief layer. Along these paths, the material resistivity was reduced by more than a factor of 100 compared to the uncontacted epitaxy. It is suggested that the cause of the additional leakage is decoration of dislocations. This result is important for understanding buffer transport, a critical parameter for breakdown, and buffer charge storage.**

***Index Terms*— AlGaN/GaN HEMT, vertical breakdown, vertical leakage, ohmic contacts.**

I. Introduction

AlGaN/GaN-on-Si high electron mobility transistors (HEMTs) are especially suited to power electronics due to their high breakdown field, high electron mobility, high carrier density, and compatibility with standard ≥150 mm Si process lines [1]. These properties allow for high voltage blocking in the off-state and low on-resistance in the on-state, resulting in highly efficient operation, all at low cost. However, there are still some challenging issues which can impact operation such as current collapse (the accumulation of negative charge in the buffer in the off-state which subsequently increases the on-resistance [2]), as well as vertical leakage in the off-state which limits the maximum operating voltage, and hence device efficiency.

Reducing the resistivity in the top layers of the epitaxy has been linked to the suppression of current collapse due to the ease with which the trapped charge can be neutralized [3]–[6]. This can be achieved, at least partially, by preferential leakage under the contacts which has been observed experimentally [7] and is routinely included in simulation [8], [9]. Although these preferential leakage paths are required for low current collapse buffers, their origin and the depths to which they extend are not fully understood. Previously suggested origins include contact spiking, metal in-diffusion and dislocation decoration [3], [7], all of which are associated with increased vertical leakage.

Increased breakdown voltage has been achieved laterally, with field plates increasing the size of the gate-drain depletion region [10], [11], and vertically by increasing the thickness of the (Al)GaN layers [12]. However, this thickness is limited by difficulties in managing the stress in GaN-on-Si growth due to the large lattice mismatch [13]. Instead, further increases in breakdown voltage can be achieved by optimizing the breakdown field of the epitaxy [14], [15]. It has been previously indicated that the choice of contact metallurgy impacts the vertical breakdown [16], with the implication that the Ti/Al based contacts (compatible with Si foundries) increased the vertical leakage. In this letter, we study the impact Ti/Al contacts have on the resistivity of the epitaxy and subsequent vertical breakdown. The quasi-static capacitance-voltage (QSCV) technique, applied to purpose designed structures, was used to measure the resistivity and depth of additional leakage paths introduced by the contacts. This is a result which is essential for full understanding of the current-transport in the semi-insulating buffer structure, responsible for breakdown and charge storage phenomena such as current collapse.

II. Experimental Details

The vertical leakage structures used in this study were fabricated using a typical AlGaN/GaN-on-Si epitaxy architecture as shown in Fig. 1a. This consists of a >1 Ωcm silicon substrate, AlGaN/GaN superlattice strain relief layer, carbon doped GaN buffer layer, unintentionally doped GaN channel and AlGaN barrier. The wafer was passivated with Al_2O_3 and SiO_2. The total thickness of the channel and GaN:C layer in this epitaxy was 1.3 μm with 1.9 μm of strain relief. The sheet resistance of the 2D electron gas (2DEG) was measured as 550 Ω/sq. Full details of the Ohmic contacting process used on this wafer have been published previously [17]. The AlGaN barrier was fully recessed followed by the deposition of Ti/Al/TiN contacts with a Ti/Al ratio of 0.05 which was annealed at only 550°C, delivering a contact resistance of ~0.6 Ωmm. All vertical leakage structures consisted of a fixed active area of 110×110 μm^2 isolated by a nitrogen implant with an energy of up to 375 keV to achieve an isolation depth of 550 nm. Inside this active area, Ohmic contacts of varying sizes were made

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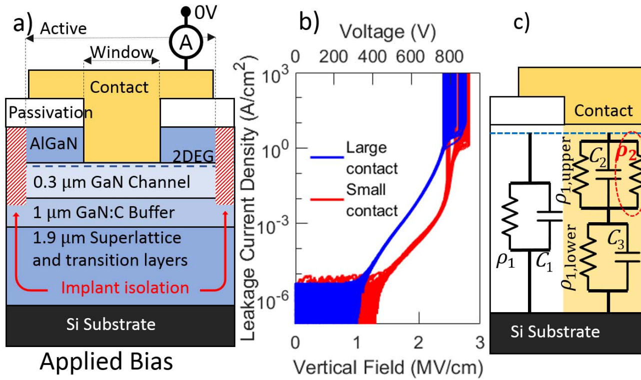

Fig. 1. a) The layout of the vertical leakage structure on a typical AlGaN/GaN epitaxy. Vertical breakdown measurements are shown in b) on structures where the contact filled the entire active area (Large contact) and also 5x5 μm^2 (Small contact). Measurement of the current density below 10^{-5} A/cm^2 was limited by the instrument. c) A lumped equivalent circuit diagram of the epitaxy treating the stack as a leaky dielectric. Under the contact, shaded in yellow, an additional leakage path with resistivity ρ_2 is included.

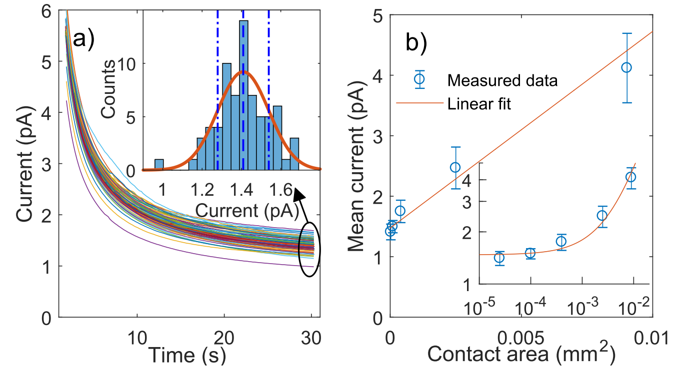

Fig. 2. a) Vertical current transients during a 200 V stress on structures with a 5×5 μm^2 contact. The distribution at 30 s is inset. b) The mean vertical leakage current for each vertical leakage structure scales linearly with contact area. The same data is inset on log-log axes of the same scale and show the standard deviation divided by the mean is approximately constant.

through windows in the passivation layer. A breakdown field of 2.7 MV/cm was measured on a structure whose window area filled the active area (Fig. 1b) demonstrating this is already an excellent buffer. Lateral conduction paths have been suppressed in this optimized buffer. This has been confirmed by the invariance of back-gate 2DEG pinch-off voltage across contacted structures with various active areas when using the Si substrate as the back-gate [3] (not shown here). The presence of lateral conduction paths (such as a 2D hole gas which can extend up to 100 μm outside the active area [18]) would have the effect of reducing the pinch off voltage in smaller active areas, but that was not seen here.

For all measurements in this letter, a negative bias was applied to the substrate and the current was measured at the surface contact which was held at 0 V. This resulted in a field over the epitaxy of the same polarity as experienced in normal transistor operation. Two measurements were performed; current transient measurements with a substrate bias of −200 V were applied to >35 of each structure geometry. The current level at 30 s was used to assess the mean vertical leakage in each structure. Sampling the current 30 s into the transient ensured that the decaying displacement current spike from the step bias did not influence the leakage current measurement. The effect of surface charging on the transient was assessed using a guard ring structure [19]. After a decay of ∼5 s, no surface effects were measurable and so this did not affect the results at 30 s. In addition, quasi-static capacitance-voltage (QSCV) measurements were performed. This technique permits the observation of dynamics which are too slow for a conventional capacitance voltage bridge. A continuous voltage ramp of −1 V/s was applied to the substrate down to −40 V and back. The current measured at the surface contact during this ramp was a sum of the leakage current and a displacement current generated by the ramp of $I_{disp} = C \cdot dV/dt$. As the sign of the displacement current depends on the direction of the ramp, by ramping in both directions, the displacement current component will change sign with the ramp direction. The measured current is always $I_{meas} = I_{leak} \pm I_{disp}$ thus these two components can be distinguished and the displacement current then be used to evaluate the quasi-static capacitance of the structure.

III. Results

The current transients from the structures with the smallest contact are shown in Fig. 2a along with the resulting distribution. A normal distribution was fitted to the data to extract the mean and standard deviation. This process was repeated for each geometry (shown in Fig. 2b), where the mean leakage current is seen to increase linearly with contact area. The ratio of standard deviation to mean was found to be largely independent of contact size, best seen on the log-log axes inset to Fig. 2b.

Following this, three structures of each geometry exhibiting mean vertical leakage were the subject of QSCV measurements. The raw measured current from the bidirectional continuous voltage ramp is shown in Fig. 3a along with the decomposition of the two constituent contributions in Fig. 3b, identified by the change in polarity with ramp direction. The mean displacement current was converted to capacitance by dividing by the ramp rate and, as shown in Fig. 3c, also monotonically increased with contact area.

IV. Model

Considering every structure has the same active area, and the contacts contact a 2DEG which extends to fill the entire active area regardless of contact area, the results of these measurements would at first sight be expected to be uniform across all geometries. However, as seen in Fig. 2b, the area of the contact has the effect of increasing the vertical leakage. This result is consistent with previous work [16] and with the ∼0.45 MV/cm shift in the vertical leakage characteristics seen at lower fields in Fig. 1b. This shift shows the presence of the contact increases the vertical leakage current, although the hard breakdown field is only decreased by ∼0.13 MV/cm, indicating the final failure mechanisms are similar. The lack of a plateau in these characteristics indicates that the leakage

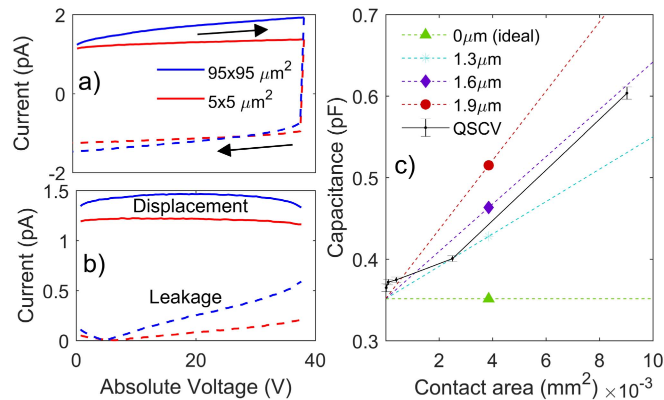

Fig. 3. a) The bidirectional continuous IV for the QSCV analysis on two different structures. This data is decomposed in b) into the displacement and leakage components based on the sign change with ramp direction. c) The capacitance of each vertical leakage structure geometry. A parallel system capacitance of 0.93 pF from an open calibration was subtracted from the results. The solid and dashed lines show the measurement data and model respectively.

did not induce deep depletion in the Si substrate, and the Si can be treated as a ground plane [20].

Although the leakage currents fit a normal distribution, since variations in the dislocation density and in the leakage path conductances would both result in a normal distribution, it is not possible to tell from the shape which one, or a combination of both are the cause.

The capacitance between 2DEG and Si substrate would equally be expected to be invariant across the structures in the absence of extended leakage paths. We propose the model shown in Fig. 1c, where a region of reduced resistivity exists below the contact due to the metallization. The equivalent circuit includes an additional leakage path (ρ_2) in parallel with the existing resistors which results in the observed increase in vertical leakage with contact area.

This model results in a quasi-static capacitance increase. The structure is represented as two parallel equivalent circuit diagrams; around the contact, the epitaxy is simplified into a leaky dielectric layer, represented by a capacitor and a resistor. Underneath the contact an additional leakage path is introduced lowering the resistivity in the upper part of the epitaxy over a certain depth. Considering a potential divider, this lower resistivity means more of the voltage is dropped over the lower part of the stack giving rise to a higher displacement current which is dependent on C_3 (since now $I_{disp} \sim C_3 \cdot dV/dt$).

As the total capacitance of the structure is the sum of the capacitance under the contacts and the capacitance in the remaining active area, the capacitance increases with contact area. The exact capacitance change resulting from this model depends on the depth that the region of lowered resistivity (represented by ρ_2) extends. The equivalent circuit was used to model the expected capacitance at various depths with the results shown in Fig. 3c. The inference is that the depth of these leakage paths extends $\sim$1.6 μm down from the contact metal, stopping in the superlattice. Transmission electron microscopy (TEM) studies of other Ti/Al based contacts indicate only 5-30 nm of metal diffusion [21], [22] and $<$ 100 nm of contact spiking [23], much less than 1.6 μm. TEM images of this particular contacting process showed no diffusion or spikes [17], which indicates a different cause. Considering the depth of these leakage paths, a more plausible possibility is the decoration of dislocations perhaps with the contact metal during annealing. These threading defects penetrate through the buffer and have been correlated with increased Ti/Al contact leakage in the past [24].

In order for this model to increase the capacitance under the contacts, the combined resistivity of $\rho_{1,\mathrm{upper}}$ and ρ_2 must be less than the effective resistivity of C_3 during the ramp. The effective resistivity of a capacitor, ρ_C, in a voltage ramp is given by

$$\rho_C = \frac{V}{\epsilon} \cdot \frac{dt}{dV} \tag{1}$$

where ϵ is the permittivity, here about $10\epsilon_0$. This places an upper bound of $\sim 10^{11}$ Ωcm on the resistivity of the upper part of the stack below the contact. The resistivity expected under the rest of the active area around the contact, ρ_1, can be calculated from the x-intercept of Fig. 2b as 5×10^{13} Ωcm, which is consistent with previous estimations for the resistivity of C doped GaN [7], [25]. This indicates more than a hundred times reduction in resistivity.

Conventional, high frequency capacitance-voltage (CV) yields the same capacitance for all structures, equal to the expected capacitance of the entire stack. This occurs since the leakage time constants are too slow to respond to the lowest available measurement frequency of 100 kHz. Therefore, $\frac{1}{RC} = \frac{1}{\rho_2 \epsilon} <$ 100 kHz which imposes a lower bound on the resistivity and results in the limits $10^7 < \rho_2 < 10^{11}$ Ωcm for $\sim$1.6 μm under the contacts.

V. Conclusions

Specifically designed structures have been used to study the effect of Ti/Al based Ohmic contacts on vertical leakage. The result of vertical leakage increasing with contact area is consistent with previous work. The key result of this study indicates that these preferential leakage paths extend $\sim$1.6 μm into the epitaxy, ending somewhere in the superlattice. These paths lower the field required for substrate leakage and appear to define the hard breakdown field. Engineering the leakage due to contacts is critical for successful high voltage device operation and managing current collapse, buffer leakage and breakdown. This result indicates that these leakage paths are much deeper than may have been expected, and this will aid accurate simulation as well as efforts to improve device performance and breakdown.

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