An Optical Content Addressable Memory (CAM) Cell for Address Look-up at 10Gb/s

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***Abstract*—We propose and experimentally demonstrate the first all-optical Content Addressable Memory (CAM) cell that comprises an all-optical monolithically integrated InP Flip-Flop and an optical XOR gate. The experimental results reveal error-free operation at 10Gb/s for both Content Addressing and Content Writing operations. The potential of these memory architectures to allow for up to 40Gb/s operation could presumably lead to fast CAM-based routing applications by enabling all-optical Address Look-up schemes.**

***Index Terms*—Optical Memories, Content Addressable Memories, Photonic integrated circuits, Semiconductor Optical Amplifiers, Optical Look-up, InP monolithic integration**

I. Introduction

The vast information density needed to be transmitted today has transformed Internet into a content-centric network requiring not only high-speed interconnections but also efficient routing platforms. Future routers need to incorporate high-speed and energy-efficient buffers to provide header parsing and Address Lookup (AL) operation directly at data line-rate, eventually also in the optical domain [1]. Fast AL becomes especially important as routing tables [2] are steadily growing in size; however its speed capabilities are still below the optical transmission line-rates. Although improved AL hardware-based solutions have been proposed [3], AL speed still remains a daunting issue with the root of the problem lying in AL's elementary hardware building blocks, i.e. the electronic Content Addressable Memory (CAM) cell.

CAMs are currently employed in most high-end routers as they offer single-clock cycle comparison of the header with all memory entries in their look-up table [4]. However, the electronic CAM cell implementations reported so far can rarely exceed a few Gb/s despite the rich variety of optimization techniques that have been introduced. Renesas Electronics introduced recently a 1.6 G searches/s (Gs/s) ternary CAM (TCAM) running at 400MHz [5], while a recent prototype based on 6T binary CAM cells has been demonstrated at 370MHz [6]. A 500MHz TCAM design has been shown in [7], while 484ps access times and 1.25 Gs/s operation cycles have been reported by using Fin-FET binary CAM cells [8]. A Magnetic Tunnel Junction (MTJ)-based TCAM cell has been proposed in [9] with a worst-case sense delay of 263ps and write time of 4ns. Flash-based TCAM cell designs have also been presented as an alternative to the conventional approaches [10]. CAM search operational speeds have improved by means of early prediction schemes reaching up to 1Gs/s throughput [11], while similar CAM architectures reported on 145ps search operation delays [12].

Despite the need for overcoming the rather slow speed of electronic CAM configurations, optics have not managed so far to enter this area. Although a rich variety of optical memories has been demonstrated in the recent years [13]-[15], a reliable CAM cell version operating in the optical domain continues to be missing from the photonics technology portfolio. This has naturally necessitated the optoelectronic conversion of the optical packet address information whenever entering the router in packet switched networks, turning header processing into the exclusive stronghold of electronics. Research attempts to ensure header processing directly in the optical domain have also relied on the use of electronic routing look-up tables, trying to retain compatibility with the AL table speeds by employing lower data rates for the optical label and exploiting different multiplexing schemes for sending the lower-rate address together with the higher-speed payload [16]. The migration path towards fast all-optical AL tables can possibly profit from the recent example of optical RAMs, where elementary optical RAM cells [15] and respective peripheral circuits have shaped a roadmap for their synthesis towards high-speed optical cache memories for Chip Multiprocessors (CMPs) [17], provided, however, that optics come up with a respective solution for the elementary AL building block, i.e. the CAM cell.

In this paper, we demonstrate for the first time to our knowledge an all-optical binary CAM cell operating at 10 Gb/s and being close to 1.5x faster than the fastest electronic CAM cell. The optical CAM cell comprises an all-optical monolithic InP FF [18] and a hybridly integrated SOA-MZI XOR gate that is used for comparing the search bit and the FF stored bit. Proof-of-concept verification is experimentally demonstrated at 10Gb/s yielding successful error-free operation for both Content Comparison and Write functionalities with 4dB and 1dB power penalty values, respectively. Taking into account the theoretically predicted speed potential of optical FFs for up to 40Gb/s [19], the proposed optical CAM cell could potentially lead to all-optical CAM bank architectures with ultra-fast AL capabilities [1].

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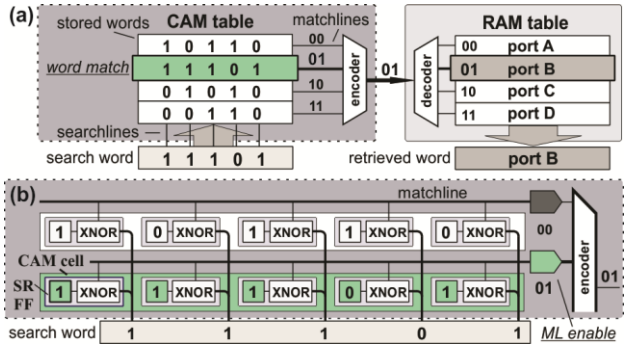

Fig. 1 (a) Implementation of AL operation based on CAM, (b) CAM table physical arrangement schematics

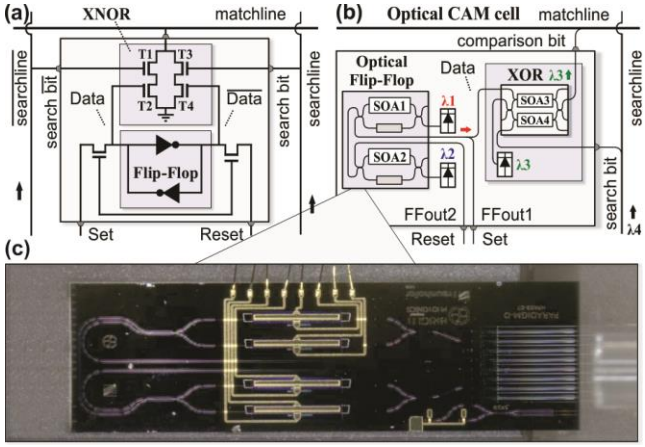

Fig. 2. (a) Electronic CAM cell , (b) Optical CAM cell , (c) InP FF chip

II. CONCEPT AND DEVICE

CAM cells employed for AL operations are usually arranged in lookup table designs, as shown in Fig. 1(a), where a CAM table unit is connected to a RAM bank. The header that accompanies an incoming data packet, hereinafter referred to as search word, is introduced to the CAM unit and gets bit-wise multicasted via the searchlines to all the CAM matchlines (ML). Every CAM matchline contains a stored word that corresponds to a certain possible address; when the stored word of a specific CAM matchline is identical to the search word, a match signal is generated to activate the corresponding CAM matchline. A matchline can be mapped to a specific RAM row by employing a proper encoding and decoding scheme, so that the activated matchline drives a RAM row enforcing a Read operation to take place. By storing the physical address of a certain router output port at a RAM row, this mechanism provides at the RAM table output the routing path on the device, referred as the retrieved word.

CAM tables are formed by several CAM matchlines configured in a parallel arrangement and having their outputs combining to a proper encoding circuit. A more detailed view of two adjacent CAM matchlines is depicted in Fig. 1(b), where each CAM matchline incorporates a number of CAM cells. Every CAM cell stores a single bit of the entire address word contained in the CAM matchline and is responsible for comparing this stored bit with the corresponding bit of the search word. This operation is called Content Comparison and the comparison result of each cell is forwarded to ML enable unit that provides the encoder with the proper word match signal. A single bit mismatch along the CAM cells comprising a CAM matchline deactivates the whole matchline implying discrepancy between the incoming search word and the word being stored at the corresponding matchline. Additional circuitry can provide the CAM table with the ability to be fully programmable for future network topology and routing rearrangements by updating the CAM cell stored values, an operation called Content Write.

In its simplest architecture among alternative designs [4], every CAM cell comprises a Set-Reset (SR) FF and a XNOR logical gate, the latter being used for bit-wise comparing the incoming search word with the FF stored value. The layout of an electronic CAM cell is shown in Fig. 2(a). The flip-flop is responsible for storing a single address bit value and its complementary signal, denoted as Data and $\overline{\text{Data}}$. The XNOR electronic gate is formed by four transistor elements, T1 to T4, that are configured as two pull-down branches between the by default precharged matchline and the ground. The XNOR gate is responsible for comparing the incoming search bit and search $\overline{\text{bit}}$ values with the $\overline{\text{Data}}$ and Data values, respectively, that are stored in the Flip-Flop, with the comparison result emerging at the matchline. Whenever a bit mismatch between the Data and search bit values is present, then either T1/T2 or T3/T4 will form a short-circuit between the matchline and the ground, forming the pull-down path for the matchline to discharge and providing in this way a logical "0" as the XNOR output. Whenever the Data and search bit values are identical, then the matchline is not allowed to discharge to ground yielding a logical "1" as the XNOR output. Whenever a new address bit value has to be stored in the CAM cell, a Write Operation is carried out by launching the new bit and its complementary value as Set and Reset signals into the Flip-Flop through the respective ports depicted in Fig. 2(a). During Write operation, the CAM cell does not yield any useful comparison functionality suggesting that Write operation should be carried out as fast as possible in order to minimize the down-time of the CAM.

The proposed optical CAM cell is depicted in Fig. 2(b). Similar to the electronic cell layout, it comprises an optical Flip-Flop that holds the stored Data and $\overline{\text{Data}}$ bit values but uses an optical XOR instead of a XNOR gate for comparing the stored Data bit with the incoming search bit emerging at the searchline. The logical XOR result appears as the comparison bit at the XOR output and is inserted into a respective matchline. The optical FF relies on a coupled SOA-MZI switch arrangement that operates in a master-slave configuration [17], powered by two CW laser sources that emit light at λ1 and λ2, respectively. Whenever a logical "0" is stored as the address bit value in the FF, the λ1 signal is dominating the optical FF yielding a logical "0" as the Data signal. Whenever the FF holds a logical "1", λ2 is the dominant signal in the FF arrangement and the λ1 signal is forced to emerge at the Data output of the FF, implying that the Data is a logical "1". The stored FF content along with its complementary value can be continuously monitored through the FFout1 and FFout2 ports, respectively. The optical XOR gate follows a conventional dual-rail optical logic XOR design exploiting a SOA-MZI switch with SOAs on both MZI branches, using a CW laser at λ3 as the input signal with the

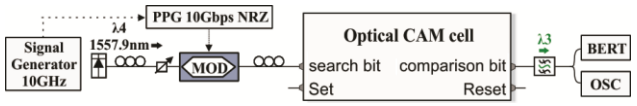

Fig. 3. Experimental setup used for Content Comparison operation at 10Gb/s

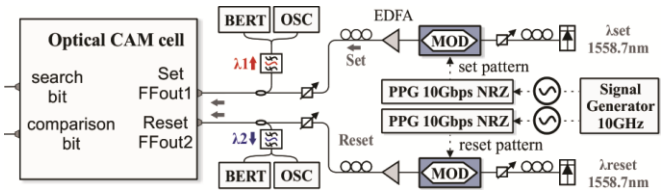

Fig. 4. Experimental setup used for Content Write operation at 10Gb/s

Data and the search bit signals serving as the two control signals that are logically XORed. Whenever the Data bit value matches the search bit carried by λ4, a logical "0" appears as the comparison bit at the XOR output and feeds the matchline. When a bit mismatch between Data and search bit occurs, then the λ3 signal emerges at the comparison bit port and a logical "1" enters the matchline. When extending the design to a complete optical CAM line that comprises several optical CAM cells, this CAM cell architecture can easily lead to a simple decision on whether all incoming search bits are identical to the respective CAM cell contents providing in this way a complete word match by logically ORing the matchline signals of all optical CAM cells along the CAM line. To this end, if all CAM cells yield a "0" comparison bit, the optical OR output will be again "0" denoting word match. If one or more CAM cells provide a logical "1" as the comparison bit at their respective matchline, then the OR operation will be again a logical "1" declaring a mismatch between the CAM line word and the incoming search word. Given that RAM row decoder and RAM bank architectures have been already demonstrated as high-speed all-optical layouts [17], bringing such multiple optical CAM-cell-based matchlines into a CAM table configuration can yield to promising optical look-up table designs following the operational characteristics of the look-up table depicted in Fig. 1(a).

To complete the functionality of the optical CAM cell by offering also Write mode capabilities, two additional optical ports are provided for allowing the new bit and its complementary value as Set and Reset signals, following the Write mechanism of coupled SOA-MZI switch FF designs.

The FF used in our optical CAM cell layout was a monolithically integrated InP optical Set-Reset FF chip, as shown in Fig. 2(c) with its electrical DC and fiber array optical I/O connections. Every SOA-MZI switch employs a 1mm long SOA at one of its branches (SOA1 and SOA2, respectively, shown in Fig. 2(b), while the second MZI branch employs a phase shifter that is used for optimally balancing the interferometer. Two optical couplers with 70/30 and 50/50 coupling ratio were used at the input and output, respectively, of every MZI switch, while coupling between the two 50/50 coupler stages of the respective MZIs was ensured through a 5mm long InP waveguide. The FF chip had a footprint of only 6x2mm^2 and was fabricated at a multi-project wafer run in the FP7 EU-funded PARADIGM project.

A hybrid silica-on-silicon SOA-MZI with one 1.6mm-lon SOA per MZI branch was used as the optical XOR gate.

III. EXPERIMENTAL SETUP

The experimental setup used for evaluating the CAM cell Content Comparison functionality at 10Gb/s is presented in Fig. 3. A 10GHz Signal Generator (SG) drives a Programmable Pattern Generator (PPG) that modulates a Ti:LiNbO3 modulator in order to produce the 10Gb/s NRZ 2^7-1 PRBS signal at λ4=1557.9nm forming the search data stream that enters the CAM cell as the control signal. The comparison result between the FF Data and the incoming search bit stream at λ3=1548nm is obtained at the respective CAM cell output and filtered in a 0.6nm 3db-bandwidth OBPF prior entering the signal quality evaluation stage that includes a Bit Error Rate Tester (BERT) and a digital sampling oscilloscope (OSC).

The device operation during Content Write functionality has been evaluated by means of the experimental setup shown in Fig. 4. A 10GHz SG drives the PPG that modulates the two LiNbO3 modulators in order to produce the 10Gb/s NRZ Set/Reset signals, both being at a wavelength of 1558.7nm. The FF content is recorded via the power levels of the output signals at λ1 and λ2 that emerge at the FFout1 and FFout2 ports of the CAM cell, respectively. These signals are filtered in a 0.6nm 3db-bandwidth OBPFs centered at λ1 and λ2, respectively, before reaching the digital sampling oscilloscope and the BERT. Erbium-doped Fiber Amplifiers (EDFA) and Variable Optical Attenuators (VOA) were incorporated in both experimental setups for power loss compensation and power level management of the signals while Polarization Controllers (PC) have been used to adjust the signal polarization state.

The two CW signals that were used to power up the two optical switches of the CAM cell FF at both operations were at λ1=1552.3nm and λ2=1553.9nm, respectively.

IV. EXPERIMENTAL EVALUATION

Fig. 5 depicts the experimental results obtained for the CAM cell Comparison and Write functionalities at 10Gb/s. Fig. 5(a)-(d) refer to the Comparison operation between the stored bit in the FF and the search bit data stream. Fig. 5(a) shows the two states of the FF corresponding to λ1 low or high powers levels, respectively, emerging at the FF out port. Fig. 5(b) shows the corresponding time traces of the PRBS 2^7-1 data stream inserted into the CAM cell as the search bit. Successful Comparison functionality at 10Gb/s can be revealed by the XOR output pulse traces shown for both FF states in Fig. 5(c). Fig. 5(d) illustrates the respective eye diagrams of the respective XOR output signals that carry the comparison outcome, having an average extinction ratio (ER) of 9.2dB. CAM cell Write mode functionality can be identified through the results presented in Fig. 5(e)-(h). Fig. 5(e) and 5(f) show the Set and Reset data pulse streams and their corresponding eye diagrams, while Fig. 5(g) and 5(h) depict the stored FF content emerging at FF out 1 and FF out 2 output ports, respectively. Successful Write functionality at 10Gb/s can be confirmed as the FFout2 and FFout1 pulse traces follow closely the content of the Set and Reset signals, respectively, when complementary logical values are carried by the Set and Reset sequences. The grey-highlighted areas in Fig. 5(e)-(h) correspond to the case where both the Set and

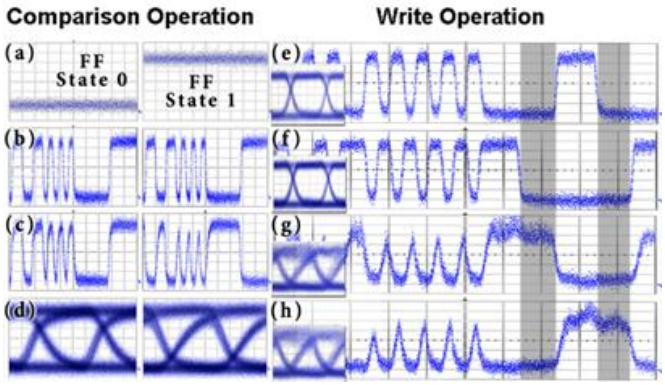

Fig. 5. Experimental results of: 10Gb/s Comparison operation (a)-(c) Time traces (200ps/div) and (d) eye diagrams (15ps/div, 10Gb/s, Write operation (e)-(h) Time traces (300ps/div) and eye diagrams (20ps/div).

Reset signals equal a logical '0' and the FF content remains unchanged retaining its last-induced logical state; a Set-induced storing is indicated in the right highlight area and a Reset-induced storing in the left one. Clearly open eye diagrams are obtained for both the FFout1 and Fout2 optical signals, revealing an average extinction ratio of 6.5dB. The CAM cell Comparison and Write operations were both verified with the aid of BER measurements. The BER diagrams in Fig. 6(a) reveal error-free Comparison Operation at 10Gb/s with a power penalty of 1dB at 10^{-9} for both CAM cell logic states. Successful Error-free operation at 10Gb/s has been obtained also during Write functionality exhibiting a power penalty of 4dB at 10^{-9}, as shown in Fig. 6(b). The power penalty during Content Comparison refers mainly to the degradations induced by the optical XOR gate, while in Write mode operation the higher power penalty value stems mainly as a result of the dynamic operation of the CAM cell FF.

For the evaluation of the Comparison operation, the average power levels of the search bit data stream, the CW input signal and the FF output entering the SOA-MZI XOR gate were 2dBm, -1dBm and 2 dBm, respectively. The two CW FF inputs at λ1 and λ2 had a power level of 7dBm and 10dBm, respectively. The SOAs of the SOA-MZI XOR gate were both electrically driven at a DC current of 250mA, while the two FF SOAs both at 270mA. During Write operation, the driving current of the two FF SOAs were 294mA and 289mA, respectively, with the Set and Reset signals having each 15dBm peak power and the two CW FF inputs (λ1 and λ2) a power level of 9.6dBm and 8.5dBm, respectively.

V. CONCLUSION

We have presented the first all-optical binary CAM cell utilizing a monolithically integrated InP FF and a hybridly integrated SOA-MZI XOR logic gate. Experimental evaluation revealed error free operation for both Content Addressing and Content Write operations at 10Gb/s showing the potential of CAM cells for large-scale integration and incorporation in efficient all-optical CAM-based AL tables.

VI. ACKNOWLEDGEMENTS

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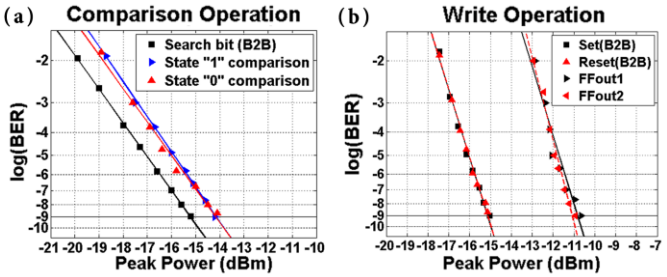

Fig. 6. BER measurements for: (a) Comparison and (b) Write operation.

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