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Thermal Transport in Superlattice Castellated Field Effect Transistors

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Abstract—Heat extraction from novel GaN/AlGaN superlattice castellated field effect transistors developed as an RF switch is studied. The device thermal resistance was determined as 19.1 ± 0.7 K/(W/mm) from a combination of Raman thermography measurements, and gate resistance thermometry. Finite element simulations were used to predict the peak temperatures and show that the three-dimensional gate structure aids the extraction of heat generated in the channel. The calculated heat flux in the castellations shows that the gate metal provides a high thermal conductivity path, bypassing the lower thermal conductivity superlattice, reducing channel temperatures by as much as 23%.

Index Terms—AlGaN, FET, Temperature

I. INTRODUCTION

GaN has a wide bandgap, high breakdown field, and high carrier mobility [1]. These desirable characteristics have led to wide ranging applications of GaN-based devices, from high-frequency, high-power RF, through to efficient DC power converters [2]. Superlattice castellated field effect transistors (SLCFETs) are a new RF switch design [3]. They benefit from a reduced on-state resistance and low off-state capacitance, resulting in a cut off frequency up to eight times higher than other FET based RF switches [4]. SLCFETs can provide the low loss, broadband performance of RF MEMS as well as the speed and reliability of FETs [5]. SLCFETs have small feature sizes and heating is localized within a channel region smaller than 160 nm, making heat extraction a challenge. If heat is allowed to build up in the small features, this can cause an increase in ON-resistance, and potentially early device failure. Here we study their thermal dissipation, which must be understood because of the potential adverse effect of channel temperature on electrical device performance and reliability.

To extract the temperatures experienced in the device, micro-Raman thermography and gate resistance thermometry (GRT) are used to determine the buffer and gate temperatures respectively. Finite element simulations are used to extrapolate

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The temperature of the device during its operation is measured and simulated, where the gate sits vertically above the channel, reproducing the superlattice only. The number of castellations was taken from literature [11], [12] to be 20 castellations.

The simulation was used to create the I(V) curve for Vg = 0 V and power density of 1.3 W/mm from the finite element simulation. 3D finite element thermal simulations were undertaken using ANSYS®. The simulation is then used to predict the channel temperature (ΔTc) at the power dissipations used in the experiments.

III. RESULTS AND DISCUSSION

Fig. 3 shows the measured Raman E2 (high) peak, which is used to calculate the temperature. Measured and simulated buffer temperatures in the devices along with the predicted temperatures are displayed in Fig. 4. All temperature increases shown are with respect to the temperature at the edge of the sample, caused by the thermal resistance between sample and its holder (Rsh). For Raman measurements the temperature measured experimentally corresponds to the temperature of the buffer layers in the device; the finite element simulation was fitted to this measurement and used to extract the peak channel temperature. The so determined average thermal conductivity for the buffer and interface layer in the thermal model was found to be 46.3 W/m.K. This agrees with thermal conductivity values for AlGaN and thermal boundary resistances for GaN-on-SiC devices reported in [11], [14].

The GRT measurement gives an average temperature along the entire gate finger, not just the active gate width of 135 µm. As shown in Fig. 1 (d) there is an additional 15 µm of gate finger outside the active area. Temperatures measured from gate resistance thermometry (ΔTGR) will therefore be lower than the peak temperature in the gate (ΔTGF). By finding the temperature profile of the gate in the simplified thermal simulation we determine

\[ ΔT_{GF} = 1.11ΔT_{GR} - 0.11ΔT_B \]  

where \( T_B \) is the temperature at the end of the gate finger. As \( R_{SH} \) cannot be determined in the GRT experimental set up, this parameter was adjusted in the thermal model to fit the experimental results. The measured \( ΔT_{GR} \), corrected \( ΔT_{GF} \) and determined channel temperature \( ΔT_C \) from these are shown,
Table I

<table>
<thead>
<tr>
<th>Device Layout</th>
<th>Gate (°C)</th>
<th>Buffer, Bottom (°C)</th>
<th>Substrate, Top (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current</td>
<td>95</td>
<td>41</td>
<td>25</td>
</tr>
<tr>
<td>GaN Buffer</td>
<td>72</td>
<td>34</td>
<td>24</td>
</tr>
<tr>
<td>Diamond Substrate</td>
<td>77</td>
<td>20</td>
<td>5</td>
</tr>
</tbody>
</table>

Finite element simulations suggest this layer causes the channel temperature $\Delta T_C$ to be 21°C hotter than the gate temperature $\Delta T_{GR}$ at 5.7 W/mm power dissipation. Reducing its thickness from 15 nm to 5 nm could reduce $\Delta T_C$ by 10%; heat flux through the gate foot is 3× larger than the heat flux through the channel foot for the 5 nm gate dielectric and only 2× larger for the 15 nm gate dielectric.

Currently, the devices differ from many traditional GaN based HEMTs in their use of an AlGaN buffer. Including aluminum increases the bandgap and hence the critical field of the buffer, however it also reduces the thermal conductivity. As shown in Table I, at 5.7 W/mm of power dissipation the finite element simulations suggest a temperature increase due to the buffer of 54°C, 47% of the overall temperature rise. Replacing the AlGaN with GaN and inputting a typical GaN/SiC thermal boundary resistance of 16 m²K/GW reduced the buffer temperature drop to 28°C, and the $\Delta T_C$ by 19% [9], [14]. If it is required to maintain the buffer specifications to preserve the electrical characteristics of the devices, then replacing the SiC substrate with a polycrystalline diamond substrate with assumed thermal conductivity of 1500 W/m.K has been shown to reduce thermal resistances by as much as 36% in GaN HEMTs. The impact is reduced in SLCFETs due to the higher thermal resistance of the buffer, for a thermal boundary resistance of 16 m²K/GW and a diamond substrate with a constant thermal conductivity of 1500 W/m.K there was still a reduction in $\Delta T_C$ of 14% [7].

**IV. Conclusion**

SLCFETs are an exciting development for efficient, reliable RF switches, but their small feature sizes mean heating is confined to nanometer scale castellations. Their thermal resistance has been found using a combination of Raman thermography, gate resistance thermometry, and finite element analysis to be 19.1 ± 0.7 K/(W/mm). Finite element analysis shows that the three-dimensional gate structure aids thermal transport, as the gold gate has a higher thermal conductivity than surrounding material and provides a heat pipe, resulting in 23% lower temperatures. When the device is operated in the saturation regime the heat deposition is focused under the gate and twice as much heat flows through the base of the gate as flows through the base of the channel. However in the linear regime, the peak temperature occurs in the access region as the gate reduces the temperature in the vicinity of the castellation. The overall thermal resistance of the device can be further enhanced by reducing the gate dielectric thickness, removing the aluminum from the buffer or using a diamond substrate.
REFERENCES


