Objective Optimization for Multilevel Neutral-Point-Clamped Converters with Zero-Sequence Signal Control

Xibo Yuan, Chenchen Wang and Yongdong Li

Affiliated Institutions:

National Key Lab of Power Systems, Dept. of Electrical Engineering, Tsinghua University, Beijing 100084 CHINA

Author information:

Xibo Yuan (corresponding author)

Address: Room 2-304, West Main Building, Tsinghua University, Beijing, China, 100084.

Email: yuanxb05@mails.tsinghua.edu.cn

Chenchen Wang

Address: Room 2-304, West Main Building, Tsinghua University, Beijing, China, 100084.

Email: wangchenchen99@mails.tsinghua.edu.cn

Yongdong Li

Address: Room 2-301, West Main Building, Tsinghua University, Beijing, China, 100084.

Email: liyd@mail.tsinghua.edu.cn

Abstract- **When the converter level count gets higher, the space vector pulse width modulation (SVPWM) will suffer from the calculation burden for synthesizing the voltage vectors and the redundant vector selection, which can be overcome by using the carrier-based PWM, as long as the carrier signal and modulation signal can be properly selected. This paper proposes a new carrier-based PWM method to achieve some important control objectives in multilevel converters by adding the optimized zero-sequence signal to the reference voltage. The control objective as well as the control method for balancing the dc-link neutral point (NP) potential is presented in the paper. Meanwhile, the relationship between the NP potential and zero-sequence voltage is comprehensively analyzed and an algorithm for injecting the optimized zero-sequence signal is derived. This paper also investigates how to use the zero-sequence voltage to achieve the "two-phase" mode operation for reducing the converter switching losses. A common mode (CM) voltage mitigation method is then proposed which effectively mitigates the CM voltage within 1/6 of the dc-link voltage. Furthermore, this paper gives a simple method to directly mapping the reference voltage to the converter switches by using the concept of voltage level. Experimental results with a scaled 1kW system validate the proposed NP potential control method and CM voltage mitigation method.**

Index Terms- **Multilevel converter, carrier-based PWM, zero-sequence signal, neutral point potential, common-mode voltage.**

1 INTRODUCTION

Multilevel pulse width modulation (PWM) converters have been developed to overcome shortcomings in solid-state switching device ratings, so that they can be used for high-power motor drives or some utility applications. The most popular structure proposed as a transformer-less voltage-source converter is the neutral point clamped (NPC) converter proposed in [1]. A three-phase three-level IGBT based diode-clamped converter is shown in Fig.1.

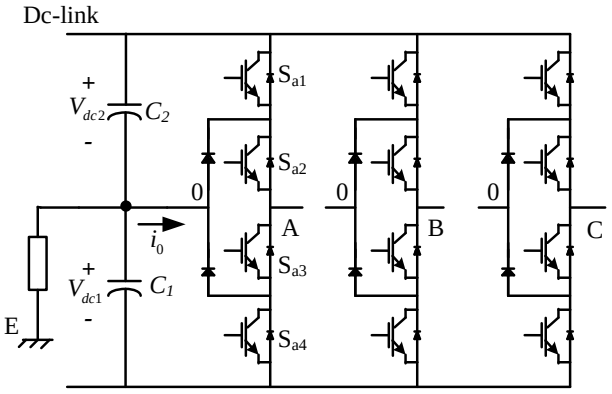


Fig.1 Structure of a three-level diode-clamped converter

The two multilevel PWM methods most discussed in the literature are multilevel space-vector PWM (SVPWM) and multilevel carrier-based PWM; both are extensions of conventional two-level PWM strategies to several levels. SVPWM is well suited for implementation on digital signal processors (DSP) and the relationship between the control objective and switching states can be synthesized and is usually very clear [2]. However, the computational burden for SVPWM increases dramatically when the converter level count gets higher, thus it becomes difficult to implement with simpler (lower cost) DSPs with limited processing capacity. Several papers have tried to reduce the calculation needs by using a new coordinate system, such as 60 degree coordinate and imaginary coordinate (line coordinate) [2-5]; however these methods still requires the coordinate transformation back and forth to synthesize the voltage vectors, and the redundant vectors selection still needs the help of a look-up table.

The basic principle of the carrier-based PWM on the other hand is to use a modulation signal compared with a carrier signal, thus generating the PWM signals to trigger the corresponding switches. It is preferable to use the carrier-based PWM since it does not need to synthesize the voltage vectors and select the redundant vectors, compared with the SVPWM, as long as the carrier signal and the modulation signal are properly selected. Past work has used various carrier signals to optimize the harmonics performance of the converter, known as alternative phase opposition disposition (APOD), phase opposition disposition (POD), and phase disposition (PD) [6,7]. This paper additionally aims to use the modulation signal to achieve some important control objectives in multilevel NPC converters.

The relationship between SVPWM and carrier-based PWM for two-level and multilevel converters can be found in [8-12], which reveals that the carrier-based PWM is equivalent to SVPWM if properly adding the zero-sequence signal (a common-mode offset signal) to the modulation signal. The redundant vector selection in SVPWM was also shown to depend on the specific type of zero-sequence signal of the equivalent carrier-based representation [10,13]. Based on this, it is possible to directly find the required modulation signal in the carrier-based PWM by analyzing the relationship between the control objective and the zero-sequence signal, thus eliminating the calculation burden of the vector synthesis and redundant vector selection in SVPWM.

Similar ideas have been used to reduce the system harmonics or improve the switch utilization [14-17], while this paper focuses on using the zero-sequence signal to control the dc-link neutral point (NP) potential, reducing the switching losses by the "two-phase" mode operation and mitigating the converter CM voltage. These three are important aspects of multilevel converters; however their relationship with the zero-sequence signal is still not well understood. Meanwhile, in this paper a simple method to modulate the converter switches by using the concept of voltage level is proposed, from which the duty cycles can be easily calculated.

The paper is organized as follows. Section 2 presents the concept of the zero-sequence signal injection and proposes a simple method to modulate the converter switches. Section 3 investigates the relationship between different control objectives (balancing the dc-link NP voltage, "two-phase" mode operation and mitigating the CM voltage) with zero-sequence signal. The control objective is achieved by properly adding the zero-sequence signal. Section 4 provides the control method verification through experiment with a 1 kW, DSP controlled, three-level NPC converter for the NP potential control method and the CM voltage mitigation method.

2 CARRIER-BASED PWM AND ZERO-SEQUENCE SIGNAL

2.1. Zero-sequence Signal Injection Concept

A universal representation of modulation signals $u_i(t)$ $(i=a,b,c)$ for three-phase carrier-based PWM can be formulated in (1) [10]

$$u_i(t) = u_i^*(t) + c_i(t) \tag{1}$$

where u_i^* is called fundamental component and c_i is called zero-sequence component. u_i^* are three-phase symmetrical sinusoidal signals, which can be either the voltage reference in the converter open-loop control or the inner current loop controller output in the closed-loop control scheme, such as vector control. The zero-sequence components c_i are injected to the three-phase modulation signal at the same time. Therefore, they do not appear in the line-to-line voltages and can be used as lever to achieve different control objectives.

In N-level NPC converters, if the negative dc-bus is set as the zero voltage reference and 1/(N-1) of the dc-link voltage is set as the base value, the phase output voltage reference with respect to the negative dc-bus can be normalized within the range of 0~(N-1) as shown in (2).

$$0 \le u_i(t) = u_i^*(t) + c_i(t) \le N-1 \tag{2}$$

Therefore, the range of zero-sequence signal which can be added to each phase is derived as

$$-u_{\min}^*(t) \le c_i(t) \le N-1-u_{\max}^*(t) \tag{3}$$

where $u_{\min}^*(t) = \min(u_a^*(t), u_b^*(t), u_c^*(t))$, and $u_{\max}^*(t) = \max(u_a^*(t), u_b^*(t), u_c^*(t))$.

The zero-sequence signal should be selected properly to be added to the modulation signal for different control objectives within the range given in (3). The concept of zero-sequence signal injection can be illustrated as in Fig.2.

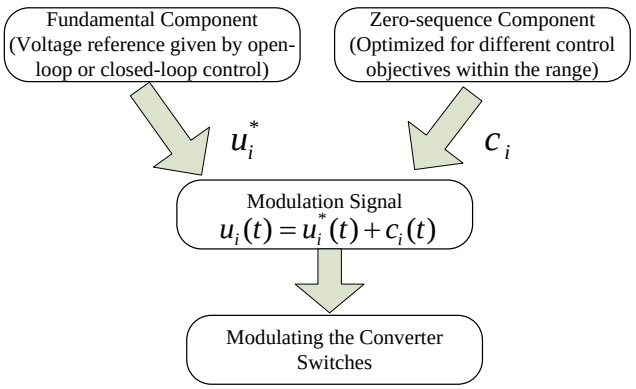


Fig.2 The concept of adding zero-sequence signal

In order to make the following analysis more clear, a three-level NPC converter is taken as an example and the converters with a higher level count can be analyzed with the same procedure. For three-level converters, N=3, with which (2) and (3) turn into (4) and (5) as shown below.

$$0 \le u_i = u_i^*(t) + c_i(t) \le 2 \tag{4}$$

$$-u_{\min}^*(t) \le c_i(t) \le 2 - u_{\max}^*(t) \tag{5}$$

2.2. Modulating the Converter Switches

An advantage of normalizing the voltage reference $u_i(t)$ using 1/(N-1) of the dc-link voltage is that it greatly simplifies the modulation of the converter switches. In three-level converters, if half of the dc-link voltage is set as the base value, the phase output voltage reference with respect to the negative dc-bus can be normalized within the range of 0~2. The integral part of the voltage reference represents the output voltage level and the fraction part will determine the duty cycle, which significantly reduces the process of calculating the converter duty cycle. Taking phase A in Fig.1 as an example, where Sa1 and Sa3, Sa2 and Sa4 will switch complementarily, if the reference voltage value is between 0~1, then the voltage level is la=0, meaning that switch Sa1 is always OFF and Sa3 is always ON; while Sa2 and Sa4 turns ON and OFF alternately based on the duty cycle. Similarly, la=1 corresponds to switch Sa2 always ON and Sa4 is always OFF, with Sa1 and Sa3 modulating. If the phase A voltage reference is 0.8, then la=0, switch Sa1 is always OFF and Sa3 is always ON, Sa2 will turn on at T1=0.1 of the switch period and turn off at T4=0.9 as shown in Fig.3, and Sa4 will operate complementarily with Sa2. The modulation of phase B and phase C follows the same process as phase A.

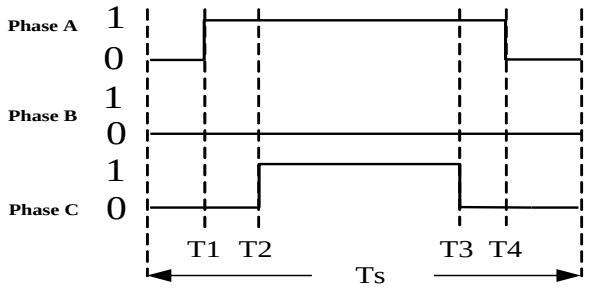


Fig. 3 Phase voltages in one PWM switching cycle

3 CONTROL OBJECTIVE OPTIMIZATION WITH ZERO-SEQUENCE SIGNAL INJECTION

3.1 Dc-link Neutral Point Potential Control Objective

NP potential control is an important issue in NPC converters, as indicated in [18, 19] and is thoroughly analyzed in [18] regarding the NP potential variation in terms of SVPWM. In the following sections, the control objective and strategies will be derived with the proposed multilevel carrier-based PWM by analyzing the relationship between the NP potential and the zero-sequence voltage.

To minimize the NP potential variation, the control objective can be set as (6)

$$\min V = \left| V_{dc1} - \frac{V_{dc1} + V_{dc2}}{2} \right| \tag{6}$$

where, V is the control objective and V_{dc1}, V_{dc2} are the dc-link capacitor voltages as shown in Fig.1. Eq. (6) implies that the lower capacitor voltage should be as close to half of the dc-link voltage as possible, thus balancing the NP potential. In each switching period, the NP potential variation ΔV_{dc1} can be calculated by

$$\Delta V_{dc1} = \frac{i_0 \times T_s}{C} \tag{7}$$

where, i_0 is the neutral current as shown in Fig.1, Ts is the switching period, and C is the dc-link capacitance value. When any phase is clamped to the NP, the neutral current flows through it varying the NP potential value. Assuming that the neutral current i_0 is constant within the switching cycle, the average neutral current during a switching period is the product of the phase current i_i (i=a,b,c) and the NP connection time duration [20,21]. The actual phase current can be measured by current sensors, and the time duration connecting to NP can be easily determined from the modulation scheme discussed above. If the integral part of the voltage reference u_i ($i = a, b, c$) is 0 (voltage level $l_i = 0$), the time duration will be the fractional part of u_i (Sa2 and Sa3 is ON). On the other hand, if $l_i = 1$, the time duration will be 1 minus the fraction part of u_i. Thus, the average neutral current can be expressed by

$$\overline{i_0} = \sum_{i=a,b,c} i_i \times ((1 - \mathrm{int}(u_i)) \times frac(u_i) + \mathrm{int}(u_i) \times (1 - frac(u_i))) \tag{8}$$

where, int(u_i) denotes the integral part of u_i and $frac(u_i)$ denotes the fractional part of the u_i in the normalized system

The control objective is to let the capacitor C_1 voltage to be as close to the half of the dc-link voltage in the next switching cycle as in (6). Now, the voltage variation of capacitor C_1 in the next switching cycle can be predicted by (7), which indicates that the NP current i_o will determine the capacitor voltage variation. From (8), it is obvious that the NP current i_o is affected by the voltage reference u_i, which can be adjusted by adding the zero-sequence voltage as indicated in (2); therefore, the control objective can be rewritten as (9) where n is the time index and the control lever is the zero-sequence voltage.

$$\begin{aligned} &\min V = \left| V_{dc1}(n-1) - \frac{V_{dc1}(n-1) + V_{dc2}(n-1)}{2} + \Delta V_{dc1}(n) \right| \\ &\textit{Constraint}: \quad -u^*_{\min}(t) \le c_i(t) \le 2 - u^*_{\max}(t) \end{aligned} \tag{9}$$

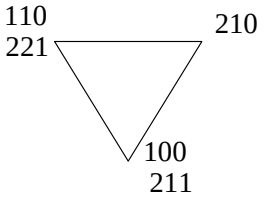
Based on the above analysis, the dc-link NP potential control scheme is described as follows: 1) In each control cycle, the three-phase currents and the dc-link upper and lower capacitor voltages are measured. The fundamental component u_i^* is given by the inner current control loop; 2) From (5), the possible zero-sequence voltage range can be calculated; 3) Search for the best zero-sequence voltage in the range that minimizes the objective in (9).

A simple way to carry out step-3 above is to evaluate several values equally distributed in the zero-sequence voltage range. Then, for each of these values c_i, the voltage reference u_i is calculated by adding it to the fundamental components u_i^*, and from (7) and (8), the NP voltage variation can be predicted and the minimum value of the objective function can be found by (9). Finally, the zero-sequence voltage leading to the minimum value of (9) is added to the fundamental component to generate the voltage reference. Note that, for N-level converters, the control objective in (6) should be chosen in such a way that each of the N-1 dc-link capacitor voltages should be as close to 1/(N-1) of the dc-link voltage as possible. Therefore, the summation of the voltage difference between each of the N-1 capacitor voltages and the 1/(N-1) of the dc-link voltages can be set as the control objective.

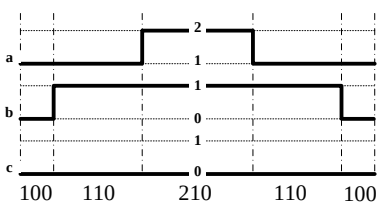
The above search method can only find the best value among the evaluated points. The control performance is affected accordingly by the number of points considered, which is limited in turn by the DSP processing capacity and the total control cycle.

3.2 "Two- phase" Mode Implementation

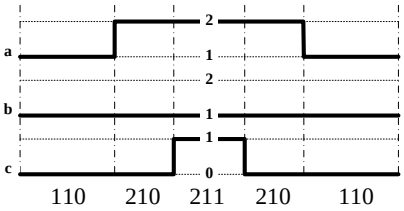
Within one PWM switching period, either all the three phases-legs operate ("three-phase" mode) or only two phase-legs operate ("two-phase" mode). The "three-phase" mode shows better harmonics spectrum and the "two-phase" mode can reduce the switching losses due to less switching actions in one switching period [10, 15]. In SVPWM, when synthesizing the reference vector, it is suggested to select the nearest three space vector (NTV) states with the middle two vectors centered in each half carrier (or equivalent) switching interval[22]. Taking a triangle in the space vector diagram in [2] for example, as shown in Fig.4(a), the possible sequences of the NTV are (100)-(110)-(210),(110)-(210)-(211),(210)-(211)-(221), where 0, 1, and 2 means that the corresponding phase output voltage is clamped to either the negative dc-bus, NP, or the positive dc-bus, respectively.



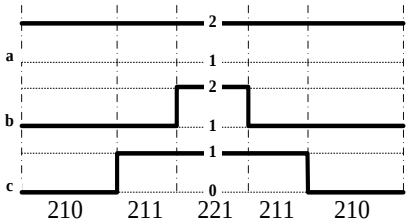
(a) One triangle of the three-level space vector diagram [2]



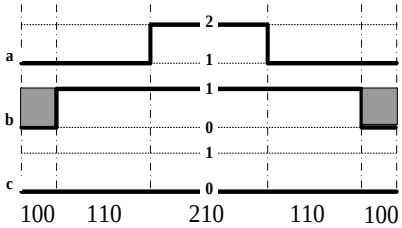
(b)



(c)



(d)



(e)

Fig.4 (a) One triangle of the three-level space vector diagram [2] ; (b)~(e) Phase voltages in one PWM switching period

The carrier-based PWM method proposed in this paper can also achieve this “two-phase” mode by properly adding the zero-sequence voltage. The zero-sequence voltage can be simply added to the phase which has maximum duty cycle each time, enabling all the possible voltage vector sequences to be covered. The value of the injected zero-sequence signal will be one minus the maximum duty cycle, to let the corresponding phase not switch.

The phase which has the maximum duty cycle can be easily located by comparing the fraction part of the reference voltage u_i. Fig.4(b)–(d) show the phase voltages in one PWM switching period corresponding to the three possible voltage vectors sequences in Fig.4(a). Fig.4(e) on the other hand illustrates how to add the proper zero-sequence voltage to get the different voltage vector sequences. In Fig.4 (b), phase B has the maximum duty cycle, if adding the shaded area (zero-sequence voltage) in Fig.4 (e) to all the three phases, then the voltage sequence changes from (b), (100)-(110)-(210), to (c), (110)-(210)-(211); thus the sequence changes equivalently to SVPWM. Next, to balance the NP potential, all the possible voltage vector sequences should be covered by properly injecting the zero-sequence voltage, searching in this way for the minimum value in (9). Then, the corresponding zero-sequence signal is added to the fundamental component finally generating the modulation signal. Note that the added zero-sequence voltage should still be within the range as in (5). In principle, the method for “two-phase” mode implementation proposed above also applies to N-level converters, where there would naturally be more possible voltage vector sequences.

It should be also noted that, if the control objective is to balance the neutral point voltage, the optimized zero-sequence voltage for balancing the dc-link neutral point potential is added. Therefore, in one switching period, all the three-phase legs may operate, which is called “three-phase” mode in the paper. The switching actions of the “two phase” mode are 2/3 as much as those of the “three-phase” mode, which can be used to reduce the switching losses.

3.3. Common Mode Voltage Mitigation

An important research topic of the multilevel converter is the mitigation or elimination of the CM voltage, which is reported to cause system problems such as motor bearing damage, insulation breakdown and electromagnetic interference (EMI) noise[23-26]. The method in [27] proposes an algorithm to eliminate the CM voltage, but at the cost of the maximum output voltage amplitude being reduced. Whereas in [28], the authors focus on minimizing the CM current via dVcm/dt control, which requires two phase-legs commutating at the same time; this in turn causes more voltage stress on the motor terminal. In [29], controlling the CM voltage by synchronizing the rectifier and inverter PWM sequence is used, but this is only applicable to the fully controllable back-to-back, rectifier/inverter systems. This paper proposes a method to mitigate the CM voltage to be within $1/6^{th}$ of the dc-link voltage without reducing the maximum output voltage by properly adding the zero-sequence voltage.

The CM voltage is defined as the voltage between the dc-link neutral point, O, and the motor or transformer neutral and can be expressed as [30]

$$V_{cm} = (V_{AO} + V_{BO} + V_{CO})/3, \tag{10}$$

where V_{cm} is the CM voltage, V_{AO}, V_{BO} and V_{CO} are the phase output voltages with respect to dc-link neutral point O as shown in Fig.1. As mentioned above, each phase-leg has three different states (0, 1, 2), denoting that the phase output voltage is clamped to either the positive dc-bus ($+V_{dc}/2$), dc-link NP (0), or the negative dc-bus ($-V_{dc}/2$) respectively. The following will derive the relationship between the CM voltage and the sum of three-phase voltage levels (the integral part of the reference voltage u_i), from where the value of the zero-sequence signal added to the three-phase voltage to mitigate the CM voltage can be determined.

The possible sum of the three-phase output voltage levels will be within the range of $0 \le (la+lb+lc) \le 4$, where la,lb,lc are the output voltage levels of phase A, phase B and phase C, respectively. Here, taking the two-phase mode for example, as depicted in Fig.3, in each switching period two phases will change their states. The CM voltages that will be generated during a switching cycle associated with the sum of the three phase output voltage levels can be calculated

by (10). In Fig.3 the sum of the voltage level (the initial state of the phase voltage) will be 0 + 0 + 0 = 0. During 0~T1, the CM voltage will be

$$((-\frac{V_{dc}}{2})+(-\frac{V_{dc}}{2})+(-\frac{V_{dc}}{2}))/3=-\frac{V_{dc}}{2}. \quad (11)$$

For T1~T2, phase A switches from 0 to 1(negative dc-bus to NP), and the CM voltage will be

$$(0+(-\frac{V_{dc}}{2})+(-\frac{V_{dc}}{2}))/3=-\frac{V_{dc}}{3}. \quad (12)$$

For T2~T3, the CM voltage will be -Vdc/6. The CM voltages that will be generated during a switching cycle associated with the possible sum of the three phase output voltage levels are summarized in Table I. As observed, only when la + lb + lc = 2, the amplitude of the CM voltages generated during the switching period will be less than or equal to $V_{dc}/6$.

In the proposed multilevel PWM algorithm, the constraint la + lb + lc = 2 is added as a constraint when selecting the zero-sequence component. Only the zero-sequence value which meets this constraint can be added to the fundamental components, thus guaranteeing the CM voltage is no larger than $V_{dc}/6$. Through this process, the expected 19 vectors are chosen from the 27 voltage vectors equivalently in SVPWM [2]. It should be pointed out that this section only aims to mitigate the CM voltage and that the NP potential may not be maintained at the same time in this case. A proper clamping method can be used to keep the dc-link NP potential balance.

TABLE I

SUM OF THE THREE PHASE VOLTAGE LEVEL AND ASSOCIATED CM VOLTAGES

Sum of three phase reference voltage level	Possible CM voltages
la+lb+lc=4	+Vdc/2 ,+Vdc/3,+Vdc/6
la+lb+lc=3	+Vdc/3, +Vdc/6, 0
la+lb+lc=2	+Vdc/6, 0, –Vdc/6
la+lb+lc=1	0 ,–Vdc/6, –Vdc/3
lb+lb+lc=0	-Vdc/6 , -Vdc/3 , -Vdc/2

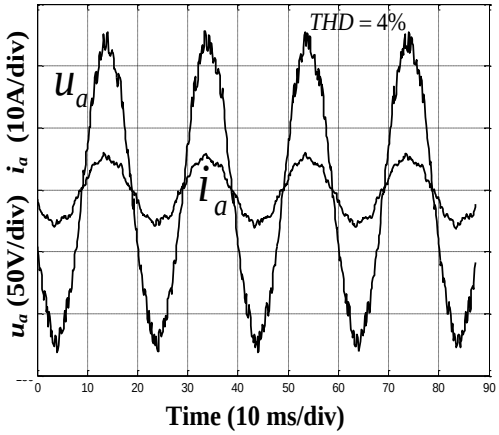
4 EXPERIMENTAL VERIFICATION

A 1 kW experimental three-level NPC prototype is built to validate the proposed NP voltage balancing scheme and the CM voltage mitigation method, which consists of switching modules, a control board, a sensor board, an input and output filter, and the load. The control board is based on the TMS320F2812 DSP.

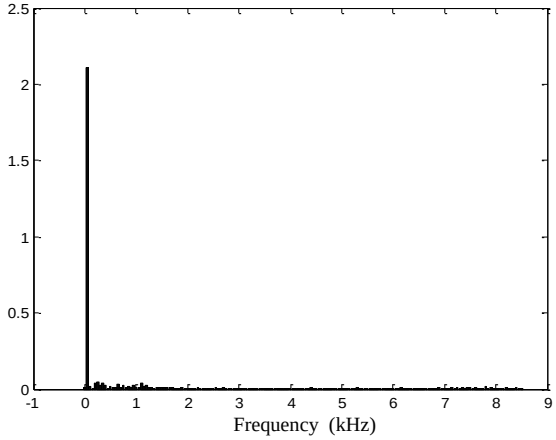
The NP potential control scheme is tested on the grid side with the system operating as an active rectifier. The system parameters are shown in Table. II. Fig.5 (a) shows the steady state input voltage and current, which achieves unity power factor and sinusoidal current and the injection of the zero-sequence voltage does not affect the rectifier normal operation. The FFT analysis of the input current is shown in Fig.5(b). Note that some low order harmonics are observed due to the use of the input variac, which is not an ideal voltage source and its leakage inductance affects the control performance. Fig. 5 (c) shows the voltage difference between the dc-link upper and lower capacitor during the rectifier steady state operation. As shown, the voltage difference is within 2V under the test condition and the dc-link NP voltage is well balanced. Specifically, the top waveform in Fig.5 (c) is using the optimized zero-sequence voltage injection and the bottom one is using the "two-phase" mode operation. The optimized zero-sequence voltage injection leads to better NP control performance and the "two-phase" mode operation achieves less switching losses compared with the "three-phase" mode since the switching actions are 2/3 as much as those of the "three-phase" mode[10][15]. Fig.5 (d) shows test results for the NP balancing algorithm with capacitor voltages intentional unbalance. The intentional unbalance is achieved by adding an offset to the measured capacitor voltage. After the capacitor voltage is unbalanced (20V difference in this case), the offset is removed at 0.11s. The NP voltage can converge to the balanced value, which validates the control algorithm. Fig.5 (e) shows the system starting dynamics for the phase current and dc-link voltage, where the dc-link voltage can reach the setting reference 245V.

TABLE II EXPERIMENTAL PARAMETERS

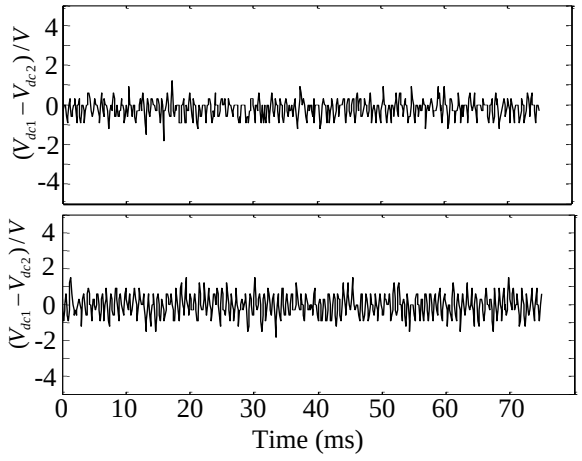
Input line voltage	170V	Dc-link capacitor value (C_1 and C_2)	270μF
Line frequency	60Hz	Switching frequency	6kHz
Dc-link voltage reference value	245V	Line inductance	5mH


THD = 4%
u_a
i_a
u_a (50V/div) i_a (10A/div)
0 10 20 30 40 50 60 70 80 90
Time (10 ms/div)

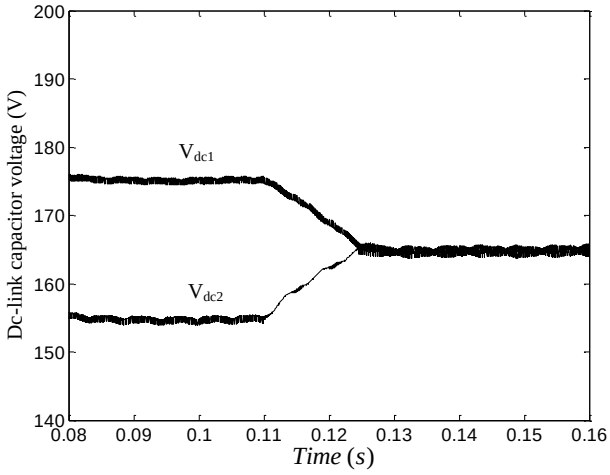
(a)


2.5
2
1.5
1
0.5
0
-1 0 1 2 3 4 5 6 7 8 9
Frequency (kHz)

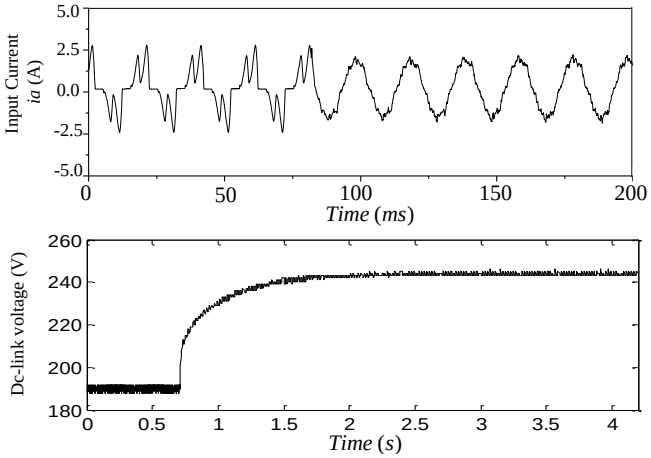
(b)


$(V_{dc1}-V_{dc2})/V$
4
2
0
-2
-4
$(V_{dc1}-V_{dc2})/V$
4
2
0
-2
-4
0 10 20 30 40 50 60 70
Time (ms)

(c)



(d)

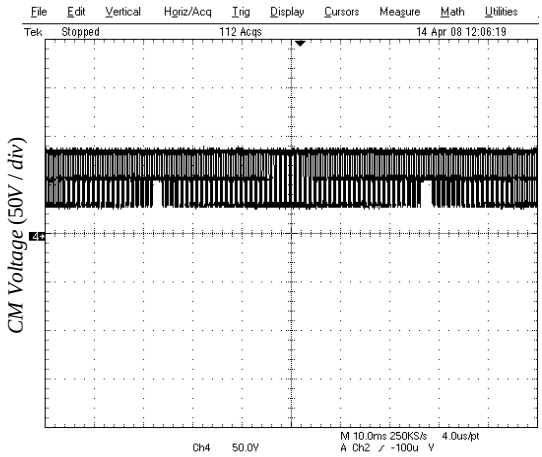


(e)

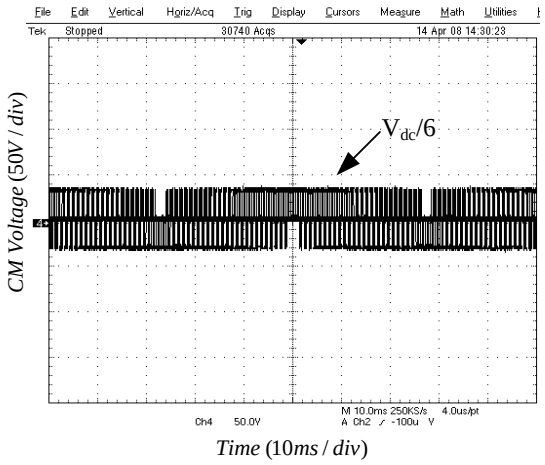
Fig.5 Experimental results with a PWM rectifier: (a) Input phase voltage u_a and input current i_a ; (b) FFT analysis of the input current; (c)Voltage difference between the upper and lower capacitor. Top trace- using the optimized zero-sequence voltage injection; Bottom trace- using the "two-phase" mode operation; (d) Capacitor voltages with intentional unbalance. (e) System starting dynamics. Top trace: input current; Bottom trace: dc-link voltage.

The algorithm for CM voltage mitigation is tested on the load side with the dc-link voltage 190 V. The load is a three-phase 1 kΩ resistor in series with a 1mH inductor. The experimental results are shown in Fig. 6, where Fig.6 (a) shows the CM voltage waveform without applying the mitigation control at a voltage frequency of 6 Hz. The CM voltage with amplitude of $V_{dc}/2$, $V_{dc}/3$, $V_{dc}/6$ (95V, 63V and 31V in this case) is apparent. Note that the CM voltage is positive, since the maximum zero-sequence voltage is added to the fundamental components. Fig.6 (b) shows that the

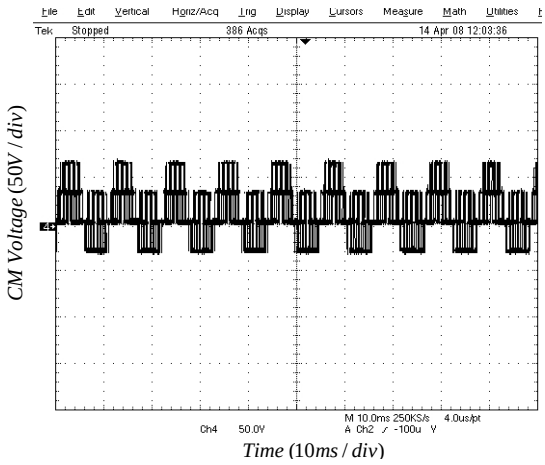
CM voltage amplitude is effectively controlled to be within $V_{dc}/6$ after the mitigation method is utilized. Fig.6 (c) and (d) show the CM voltage without and with the mitigation method at a voltage frequency of 30 Hz. The CM voltage is also effectively mitigated within 1/6 of the dc-link voltage, further validating the proposed control algorithm.



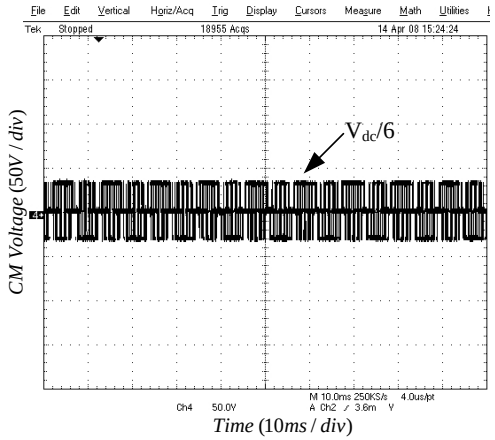
(a)



(b)



(c)



(d)

Fig.6 Experimental CM voltage waveforms (a) Output voltage frequency of 6Hz without CM voltage mitigation; (b) Output voltage frequency of 6Hz with CM voltage mitigation; (c) Output frequency of 30Hz without CM voltage mitigation; (d) Output frequency of 30Hz with CM voltage mitigation

5. CONCLUSION

This paper shows that the zero-sequence signal can be used to achieve different control objectives in multilevel NPC converters, such as controlling the NP potential, the "two-phase" operating mode, and CM voltage mitigation. The impact of the zero-sequence voltage on the NP potential was summarized in this paper under different conditions. The optimized zero-sequence voltage required to balance the NP potential was then derived. The proposed new carrier-based multilevel converter PWM method significantly simplifies the calculation complexity in SVPWM by finding the relationship between the control objective and zero-sequence signal, and the reference voltage is directly mapped to the converter switches. The proposed method and analysis can also be extended for N-level converters. A 1 kW DSP-controlled three-level experimental prototype was used to verify the proposed modulation and control algorithm.

Acknowledgement

The authors would like to thank Dr. Rolando Burgos for his comments and suggestions.

REFERENCES

[1]A. Nabae, I.Takahashi and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Applicat.*, vol.IA-17, pp. 518-523, Sept./Oct. 1981.

[2]N. Celanovic, D. Boroyevich, "A fast space vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Applicat.*, vol.31, no. 2, pp.637-641, Oct. 2001.

[3]D. Peng, F. C. Lee and D. Boroyevich, "A novel SVM algorithm for multilevel three-phase converters," in *Proc. IEEE PESC'02 Conf.*, vol.2, pp.509-513, Jun. 2002.

[4]J. Hyeong Seo, C. H. Choi, D. S. Hyum, "A new simplified space-vector PWM method for three-level inverters," *IEEE Trans. Power Electron.*, vol.16, no.4, pp.545-550, Jul. 2001.

[5]L. Yongdong, G. Yue, H. Xuan, "A general SVM algorithm for multilevel converters considering zero-sequence component control," in *Proc. IEEE IECON'05 Conf.*, vol.2, pp. 508-513, Nov. 2005.

[6]G. Carrara, S. Gardella, M. Marchesoni, R. Salutari and G. Sciutto, "A new multilevel PWM method: a theoretical analysis," *IEEE Trans. Power Electron.*, vol.7, no.3, pp.497-505, Jul.1992.

[7]R. Naderi and A. Rahamati, "Phase-shifted carrier PWM technique for general cascaded inverters," *IEEE Trans. Power Electron*, vol.23, no. 3, pp.1257-1269, May 2008.

[8]V. Blasko, "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods," *IEEE Trans. Ind. Applicat.*, vol.33, no.3, pp.756-764, Jun. 1997.

[9]F. Wang, "Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters" *IEEE Trans. Ind. Applicat.*, vol.38, no.2, pp.500-506, Mar. 2002.

[10] K. Zhou and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis", *IEEE Trans. Ind. Electron.*, vol.49, no.1, pp.186-196, Feb. 2002.

[11] D. Chung, J.Kim, S.Sul. "Unified Voltage Modulation Technique for Real-Time Three-Phase Power Conversion," *IEEE Trans. Ind. Applicat.*, vol.34, no.2, pp.374~380, Mar. 1998.

[12] D.G. Holmes and T.A. Lipo, Pulse Width Modulation for Power Converters. New York: Wiley, 2003.

[13] W. Chenchen, L. Yongdong, X. Xi, "A unified SVM algorithm for multilevel converter and analysis of zero-sequence voltage components," in *Proc. IEEE IECON'06, Conf.*, vol.3, pp. 2020-2026, Nov. 2006.

[14] L. M. Tolbert, T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Trans. Ind. Applicat.*, vol.35, no.5, pp.1098-1107, Sept. 1999.

[15]T. Bruckner, D. G. Holmes, "Optimal pulse-width modulation for three-level inverters" *IEEE Trans. Power Electron.*, vol.20, no.1, pp.82-89, Jan. 2005.

[16]J. Li, A.Q. Huang, Z. Qian, H. Zhao, "A novel carrier-based PWM method for 3-level NPC inverter utilizing control freedom degree," in *Proc. IEEE PESC'07 Conf.*, vol.1, pp. 1899-1904, Jun. 2007.

[17]B.P. Mcgrath, D. G. Holmes, T. Meynard, "Reduced PWM harmonic distortion for multilevel inverters operating over a wide modulation range" *IEEE Trans. Power Electron.*, vol.21, no.4, pp. 941-949, Jul. 2006.

[18]N. Celanovic, D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters" *IEEE Trans. Power Electron.*,vol.1,no.2, pp.242-249, Mar.2000.

[19] F. Wang, "Multilevel PWM VSIs: Coordinated control of regenerative three-level neutral point clamped pulse-width-modulated voltage source inverters," *IEEE Ind. Applicat. Mag.*, vol.10, no.4, pp.51-58 Jul./Aug. 2004.

[20] J. Steinke, "Switching frequency optimal PWM control of a three-level inverter," *IEEE Trans. Power Electron.*, vol.7, no.3, pp. 487-496, Jul.1992.

[21] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," *in Proc. IEEE IAS'93 Conf.*, vol.2, pp.956-970, Oct. 1993.

[22] B.P. McGrath, D. G. Holmes and T.A. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron.*, vol.18, no.6, pp.1239-1301, Nov. 2003.

[23] A. Jouanne, P. Enjeti, and W.Gray, "Application issues for PWM adjustable speed AC motor drives," *IEEE Ind. Applicat. Mag.*, vol. 2, pp.10-18, Sept./Oct.1996.

[24] J.M. Erdman, R.J.Kerkman, D.W.Schlegel, and G.L.Skibinshki, "Effect of PWM inverters on AC motor bearing currents and shaft voltage," *IEEE Trans. Ind. Electron.*, vol.32,no.2, pp. 250-259, Mar. /Apr. 1996.

[25]E. Zhong and T.A. Lipo, "Improvements in EMC performance of inverter-fed motor drives," *IEEE Trans. Ind. Applicat.*, vol. 31, no.6, pp.1247-1256, Nov./Dec. 1995.

[26] F. Wang, "Motor shaft voltages and bearing currents and their reduction in multilevel medium-voltage PWM voltage-source-inverter drive applications" *IEEE Trans. Ind. Applicat.*, vol. 36, no.5, pp.1336-1341, Sep./Oct. 2000.

[27] H. Zhang, A.Jouanne, S. Dai. , "Multilevel inverter modulation scheme s to eliminate common-mode voltages" *IEEE Trans. Ind. Applicant.*, vol. 36, no. 6, pp. 1645-1653, Nov./Dec. 2000.

[28] A. Videt, P.Le Moigne, N.Idir. "A new carrier-based PWM for the reduction of common mode currents applied to neutral-point-clamped inverters" in *Proc. IEEE APEC'07 Conf.* pp.1224-1230, Mar, 2007.

[29] H. Lee, and S.Sul. "Common-Mode Voltage Reduction Method Modifying the Distribution of Zero-Voltage Vector in PWM Converter/Inverter System" *IEEE Trans. Ind. Applicant.*,vol. 37, no. 6, pp 1732-1738, Nov./Dec. 2001.

[30] M. Cacciato, A. Consoli, G.Scarcella "Reduction of common-mode currents in PWM inverter motor drives" *IEEE Trans. Ind. Applicat.*, vol.35, no.2, pp. 469-476, Mar. /Apr. 1999.