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# A Software and Hardware Evaluation of Revolutionary Turbo MIMO OFDM Schemes for 5GHz WLANs

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***Abstract*—Globally, WLANs operating in the 5GHz band have been standardized by the IEEE (North America), ETSI (Europe) and ARIB (Japan). A harmonized physical layer is specified offering up to 54 Mbits/s using rate adaptive Coded Orthogonal Frequency Division Multiplexing (COFDM). Multiple Input Multiple Output (MIMO) antenna architectures coupled with Soft Input Soft Output (SISO) iterative decoding algorithms represent a revolutionary approach to the design of WLANs. At present, these techniques are the subject of intense theoretic research. In this contribution, the performance of a newly proposed iterative MIMO-OFDM architecture is explored using MIMO channel data captured in the 5GHz band. Theoretically, this technology has the potential to significantly increase future WLAN data rates. However, little practical evaluation has been reported in the literature. To address this situation, this paper describes the construction of a broadband 5GHz MIMO-OFDM test-bed. This advanced baseband/RF platform will be used in the future to evaluate emerging MIMO-OFDM WLAN architectures.**

## I. Introduction

This paper aims to enhance the current generation of 5GHz WLAN standards [1] by the application of MIMO antenna architectures and SISO iterative decoding algorithms. To date, the vast majority of studies have been performed theoretically with little regard for practical limitations and realities, e.g. the effects of mutual coupling across antennas, phase noise distortion and imperfect channel estimation. To overcome this situation, the design and construction of a broadband 5GHz flexible MIMO-OFDM test-bed is described. The platform will enable new WLAN architectures to be evaluated using hardware operating in the 5GHz band. To complete the paper, a newly proposed MIMO-OFDM architecture incorporating iterative decoding is evaluated using channel data captured from candidate antenna arrays.

## II. Hardware Test Bed

A universal software-programmable hardware simulator has been constructed. The simulator functions by transmitting modulated data sequences stored on the hard disk drive (HDD) of a PC, and storing the captured received waveforms on the HDD of a second PC. In this way, the need for real-time processing of the raw source data and the received waveforms is avoided [2] (see Fig. 1). The simulator was designed with the latest WLAN standards in mind, and can be used to simulate the physical layer of Hiperlan/2 or 802.11a.

The sampled data is transmitted at the system specified rate in real time, by the addition of a buffer between the HDD and the RF section. This simplifies the construction of the simulator enormously, without compromising the validity of the results gained. Whilst the data transmission is real-time, the duty cycle of the simulator is low to allow for HDD access. The simulator also has a novel architecture that facilitates perhaps the most interesting application, that of arbitrary MIMO system simulation. This has been achieved by combining high performance data interfaces into the hardware, allowing any number of boards to be daisy-chained from a central processor (see Fig. 2). This is essential in the receiver, where the received waveforms from every antenna are required by the processor executing the MIMO decoding algorithms. At the transmitter, the architecture merely simplifies the signal processing.

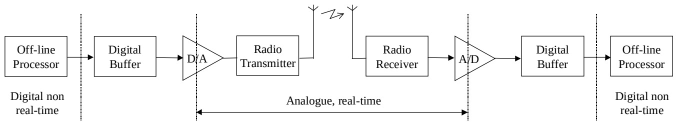


Fig. 1. System Overview

The test-bed will be used in the first instance in a large modern office in the University of Bristol. The aim is to compare its performance to software simulations that used measured channel responses recorded in the same environment. This will allow a detailed evaluation of algorithm performance in the presence timing offset errors, frequency offsets and imperfect channel state information.

The simulator hardware consists of several parts:

### *A. Baseband section*

This part of the system is the interface between the PC processor and the RF units. The section consists of a printed circuit board (PCB) per antenna element with an associated DSP (a TI ‘C6711DSK). The PCB carries a FIFO (used to buffer the data transfers into and out of the DSP), a dual interpolating DAC (used in the transmitter), a dual ADC (used in the receiver), both of 10 bit resolution, and the data interface between boards. The data interface is a Low Voltage Differential Signaling (LVDS) serial link with a data rate of 400Mbits/s, and uses Unshielded Twisted Pair (UTP) Ethernet cables to provide a controlled transmission media between boards. Also included are analogue buffers and low pass filters for signal reconstruction and alias rejection. The digital baseband daughter board is shown in Fig. 3.

A slightly modified version of this circuit board allows a TI ‘C6201 EVM DSP to control the whole system, and also to provide the data interface from the PC to the simulator. The PCI bus used in the EVM transfers data efficiently from the PC HDD to the EVM (see Fig. 2). The data is then sent from this central DSP to each of the others in turn. At each transmitter the DSP will have the data to be transmitted from that antenna only. The receiver is a dual of the transmitter architecture – data is sampled into each DSP and then sent sequentially back to the PC for storage and/or processing. Critically, all units sample data simultaneously (rather than sequentially), negating the effect of the radio channel changing over time that would otherwise result in less accurate performance estimation.

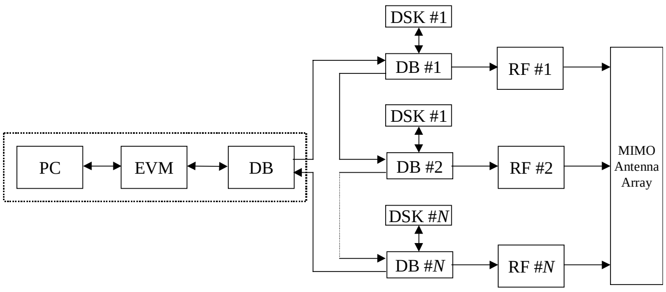

Fig. 2. Transmitter System

The whole system is kept synchronized by the DSP software which runs on each processor. The software also controls the baseband hardware, and handles all data transfers for all I/O devices in the system. Additionally, the DSP software performs various data processing tasks, although the bulk of this is done in the PC as the software complexity is much lower.

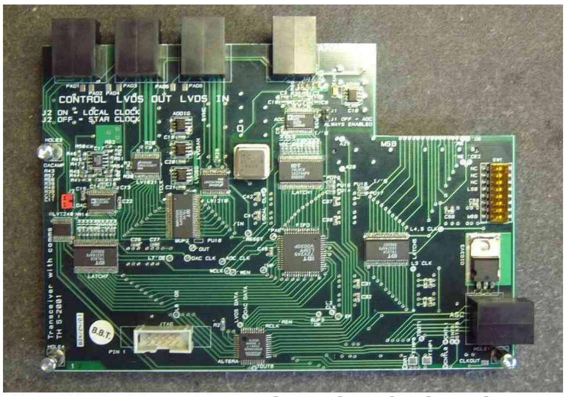

Fig. 3. MIMO Test Bed Digital Baseband Board

## B. *RF section*

A set of radio transceivers has been constructed. It is necessary to use one transceiver per antenna, as the system transmits and receives simultaneously across all antennas. Each transceiver takes in bandlimited I & Q analogue waveforms and up-converts these signals to a 5.2GHz centre frequency via one IF. Each unit similarly down-converts from 5.2GHz to quadrature baseband, with the option of applying a digital AGC to the signal.

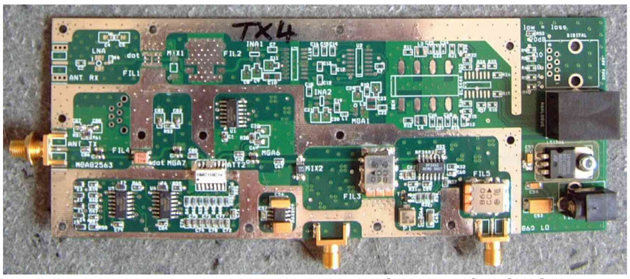

Fig. 4. Transceiver unit (transmitter chain populated only)

The output power of the transmitter is around +7dBm, and the sensitivity of the receiver approximately –85dBm. This gives a theoretical free space operating range of up to 200m, assuming 0dBi antennas and the lowest order sub-band modulation. Fig. 4 shows one of the units, assembled as a transmitter (the receive components are not fitted).

## C. *Antennas*

Circular and linear arrays of 8 elements have been developed based upon printed dipole technology. The dipoles operate at a centre frequency of 5.2 GHz and have a bandwidth of around 10%. They are printed on low cost dielectric with half-wavelength spacing at 5.2 GHz (see Fig. 5). In addition, printed antennas based upon stacked patch technology have been deployed (Fig. 6). These antennas are dual polarized wideband radiating elements devices with bandwidth of up to 20%.

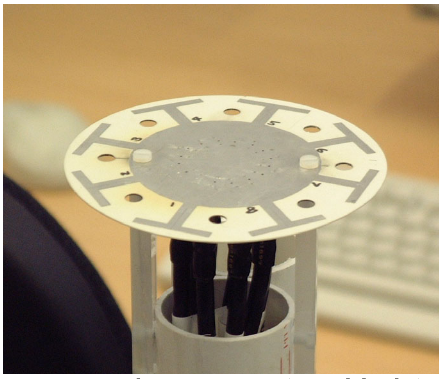
Fig. 5. Typical antenna system (printed dipoles)

Fig. 6. Typical antenna system (dual polarized patches)

## III. Channel State Information Acquisition and Timing Recovery

The beginning of each frame is preceded by a known preamble that contains data elements from a set of orthogonal matrices (see Fig. 7). For the 4 transmit antenna case, these matrices are of size 4 by 4 and are generated for each data bearing subcarrier. Based on these data elements, Channel State Information (CSI) and timing recovery is performed.

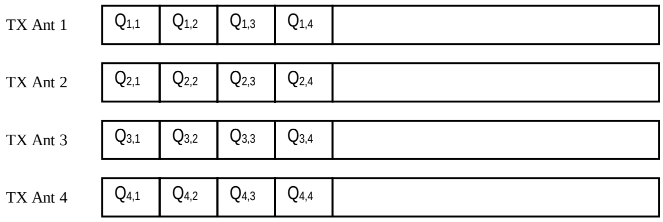


Fig. 7. Proposed preamble for the Test bed

### *A. Channel State Information Acquisition*

The elongated structure of the proposed preamble comprises 4 OFDM symbols for each transmit antenna (16µs) and provides good resilience towards noise, as an SNR gain of 6dB is achievable in the CSI estimation. Since each subcarrier is orthogonal across the OFDM symbols, $P$ and transmitters 1 to 4, the CSIs for the $k^{\text{th}}$ subcarrier is acquired through the process given by:

$$\mathbf{H}_k = \mathbf{Y}_k \mathbf{Q}_k^H$$

where $\boldsymbol{Q_k}^H$ is the Hermitian transpose of the frequency domain $\boldsymbol{Q_k}$ matrix with elements $[q_{k,i,,j}]$ where $i$; $1 \le i \le 4$ and $j$; $1 \le j \le 4$. $\boldsymbol{Y_k}$ is the vector of received symbols, $\boldsymbol{Y_k} = [Y_1\ Y_2\ Y_3\ Y_4]^{\mathrm{T}}$ and $\boldsymbol{H_k}$ is the matrix of estimated channel values.

### *B. Timing Recovery*

Time synchronization is performed on each of the Q-preambles for each respective antenna. The algorithm presented here utilizes a "windowing method" on the autocorrelation values acquired from the preamble. An 800ns window slides across the autocorrelation period of 3.2µs (the useful symbol period) and the final timing is dependent on the maximum value given by $R'_{yy}(\tau')$. The correlator output is given as:

$$R_{yy}(\tau) = \frac{1}{K_{corr}} \int_{t=-1600ns}^{1600ns} y_c(t)\hat{y}_c^*(t-\tau)dt$$

where $y_c(t)$ and $\hat{y}_c^*(t-\tau)$ represent the original and conjugate delayed version of the received Q preamble signal for each antenna. The integrator output is given as:

$$R'_{yy}(\tau') = \frac{1}{K_{\text{int}}} \int_{\tau=0ns}^{800ns} R_{yy}(\tau-\tau')d\tau$$

where $K_{int}$ represents a constant used to normalize the windowed energy to a maximum value of one. The peak of this curve corresponds to the value of τ for which the desired signal is greatest.

## IV. Turbo-BLAST-OFDM

Since their spectacular debut in Turbo codes [3], iterative decoding techniques have taken a prominent place in the quest for high promised capacities. Iterative (Turbo) detection splits the global estimation process into smaller more tractable sections that supply each other with appropriate *a priori* probability density functions. Although rigorous convergence analysis is yet to be established, overwhelming empirical evidence justifies huge interest and stimulates further research. The Turbo-MIMO-OFDM architecture [4] is a turbo version of V-BLAST OFDM proposed in [5]. It can also be viewed as a multi-carrier version of turbo bit-interleaved coded modulation with transmit and receive diversity [6] and Turbo Blast of [7].

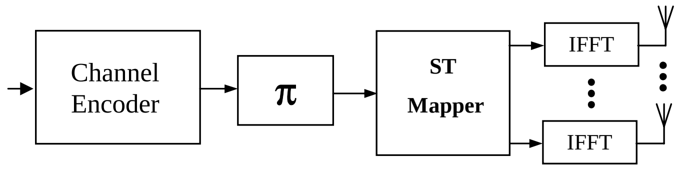


Fig. 8. Schematic of the encoder of Turbo MIMO-OFDM

The transmitter is depicted in Fig. 8. A binary stream of data $\{b_t\}$ is first transformed by a channel encoder to obtain an encoded (redundant) sequence $\{d_t\}$. Typically, convolutional or low density parity check (LDPC) coding schemes are used for that purpose. The encoded sequence is multiplexed, interleaved and then mapped to the modulation symbols (e.g. QPSK, 16-QAM etc.). The modulation symbols are then mapped to the antennas $\{s_t^{1:N_T}\}$, transformed by the IFFT pre-coders and sent by multiple antennas.

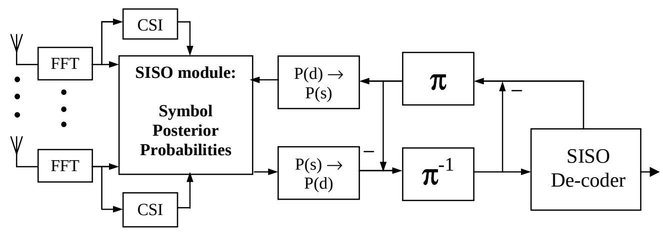


Fig. 9. Schematic of the decoder of Turbo MIMO-OFDM.

The receiver shown in Fig. 9 consists of two major soft-input-soft-output (SISO) blocks. The first accepts observations from all the antennas $\{y_t^{1:N_R}\}$ and calculates a set of marginal posterior distributions $f\left(s_t \middle| y_t^{1:N_R}, H_{t,k}, \sigma^2\right)$. This block also accepts prior distributions provided by the second block $f(s_t)$- SISO channel decoder. The channel decoder relies only on the posterior distributions produced by the first block (there is no additional prior). For the turbo system to work properly, the prior information that is supplied to the first SISO module has to be removed from the posterior distributions. This is illustrated in Fig. 9 by a branch traversing the turbo loop before the interleavers. The second branch ensures that only the so-called *extrinsic* part of the posterior distribution is handed over to the first SISO block for the next iteration. The extrinsic information is the "extra knowledge" about the data distribution gleaned through the decoding process.

The first SISO block calculates the appropriate posterior densities by enumerating amongst all points in the state-space. The whole procedure in accomplished in three steps:

1. Calculate the un-normalized joint posterior symbol density according to:

$$f\left(s_1,\ldots,s_{N_T}\middle|\mathbf{y}_k,\mathbf{H}_k,\sigma^2\right)\propto \exp\left[\frac{-\left\|\mathbf{y}_k-\mathbf{H}_k\mathbf{s}_k\right\|^2}{\sigma^2}\right]\prod_i f_i(s_i)$$

2. Normalize the joint posterior symbol density and calculate marginal densities for the symbols

$$p\left(s_i\middle|\boldsymbol{y}_k,\boldsymbol{H}_k,\sigma^2\right)=\iiint_{-i} p\left(s_1,\ldots,s_{N_T}\middle|\boldsymbol{y}_k,\boldsymbol{H}_k,\sigma^2\right)ds_{-i}$$

where $s_{-i}$ stands for all *s* except $i^{th}$.

3. Transform symbol marginal densities to bit marginal densities using:

$$\Lambda_{i,k}=\log\frac{\sum_{S_i:d_{i,k}=0} p\left(s_i\middle|\mathbf{y}_k,\mathbf{H}_k,\sigma^2\right)}{\sum_{S_i:d_{i,k}=1} p\left(s_i\middle|\mathbf{y}_k,\mathbf{H}_k,\sigma^2\right)}$$

The last point of the calculation requires the use of a modulation-labeling table.

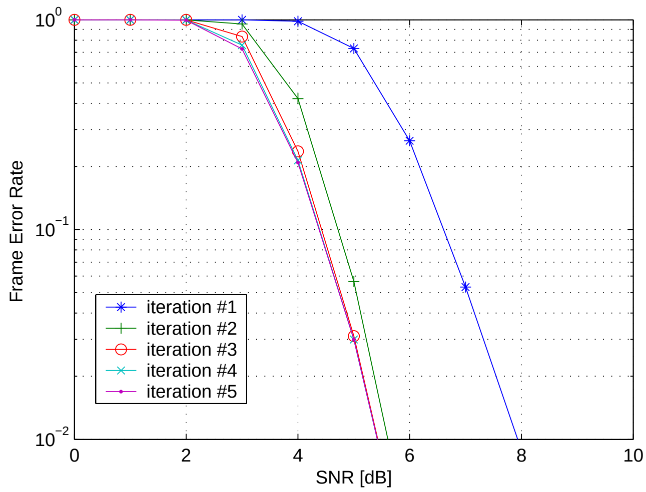


Fig. 10. Performance of MAP (Enumerator) MIMO-OFDM turbo decoder with enhanced IEEE 802.11a over measured channels - indoor environment (4 Tx by 4 Rx, QPSK, block length 960 bits, channel code RSC rate 1/2, random interleavers)

A major advantage of Turbo MIMO-OFDM is its flexibility. Most of the detection chain remains unchanged and retains the same complexity regardless of the number of antennas used, the frame length or indeed the modulation format. The only affected part is the first SISO block. The complexity of the SISO front end can be very sensitive to the number of Tx antennas and modulation format. The optimal strategy (from a performance viewpoint) involves enumerating amongst all possibilities (MAP decoding). This can lead to gigantic complexity e.g. 4,294,967,296 states for 8 Tx antennas and 16-QAM modulation. Currently, there is tremendous interest in the research community in reducing this burden.

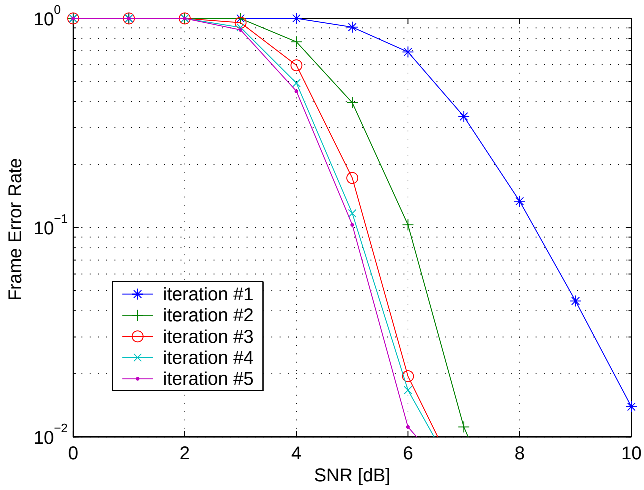


Fig. 11. Performance of MAP (Enumerator) MIMO-OFDM turbo decoder with enhanced IEEE 802.11a over synthetic (simulated) channels – ETSI H/2 model A (4 Tx by 4 Rx, QPSK, block length 960 bits, channel code RSC rate 1/2, random interleavers)

The wideband MIMO measurements utilized here have been taken using a customized Medav RUSK BRI vector channel sounder operating in the 5.2 GHz band with a bandwidth of 120 MHz. Some of the results are depicted in Fig. 10, where the performance of the enhanced IEEE802.11a standard (4 transmit and 4 received antennas) operating in an indoor environment has been investigated. Fig. 11 depicts the same system operating over simulated channels. The simulated channels are constructed from independent realizations of ETSI Hiperlan/2 channel A. In both cases results for the first 5 iterations are plotted and ideal CSI is assumed to be available. As expected, the performance improves with the number of iterations. A difference of approx. 1 dB can be observed between the simulated and the measured case. Although, in the case of the simulated channels, the improvement after the second iteration is negligible, however in the case of measured channels the second, third and fourth iteration improves performance.

## V. Future Work

The hardware simulator is flexible and will be used to investigate MIMO-OFDM architectures consisting of various numbers of transmit and receive antennas and different antenna types (including dual polarized elements) in a number of different environments. Off-line processing means that the received data sequences can be rigorously processed to evaluate various coding/decoding schemes in addition to extracting information about the effect of multiple parameters on data transmission. Such parameters might include the effect of the multipath radio environment, frequency, phase and timing offsets between the transmitter and receiver, imperfect DACs, ADCs and analogue filters in the hardware.

The test-bed waveforms are software generated and are not limited to OFDM transmissions. Within the capabilities of the test-bed (e.g. SNR achievable and bandwidth / sample rate) there are no restrictions placed on the parameters of the system under test. Thus, it is possible to simulate single carrier and W-CDMA systems by generating the required waveforms in software. Although currently the system only operates at 5.2GHz, this is not a fundamental restriction but one made to simplify the construction of the RF units and to investigate WLAN performance in this band. Also within its capabilities are simpler transmit and/or receive multi-element schemes, such as transmit and receive diversity. The hardware simulator can be expanded to handle an increased number of transmit and receive antennas (>4) by addition of identical hardware to that currently described.

An upgraded version of the hardware simulator is envisaged that will be capable of shorter cycle times and thus be able to achieve near real-time operation.

## VI. Conclusions

This paper has described a universal software-programmable hardware simulator. The test-bed has demonstrated the *real-time* transmission over an indoor radio channel of MIMO-OFDM WLAN data at 5.2GHz. The processing of the received waveforms is performed in non real-time. With further optimization, near real-time processing of results will be possible in the foreseeable future.

## Acknowledgements

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