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SNDR Sensitivity Analysis for Cascaded ΣΔ Modulators

James Morizio, Michael Hoke, Taskin Kocak, Clark Geddie, Chris Hughes,
John Perry, Srinadh Madhavapeddi, Michael Hood, Ward Huffman

Mitsubishi Electronics America - Electronic Device Group, Durham, NC 27704

Takashi Okuda, Hiroshi Noda, Yasuo Morimoto, Toshio Kumamoto,
Masahiko Ishiwaki, Harufusa Kondoh, Masao Nakaya, Takahiro Miki

Mitsubishi Electric Corporation - System LSI Division, Hyogo 664-8641 Japan

Abstract

Cascade, single and multi-bit, ΣΔ architectures provide stable, high order quantization noise shaping used in high resolution A/D conversion. One major disadvantage of cascaded ΣΔ topologies is the extreme SNDR sensitivity to gain mismatch between the analog modulator and the digital error correction logic. This paper will investigate this SNDR sensitivity phenomenon for a 6th order, 1-bit quantizer and 4th order, 5-bit quantizer cascaded ΣΔ A/D system. Circuit parameters of the switched capacitor integrator such as amplifier open loop gain, integrator gain, and amplifier offsets and layout parasitics will be characterized.

1. Introduction

Cascaded ΣΔ modulators achieve stable, higher order noise shaping with reduced oversampling rates[1,2]. These modulator topologies consist of a series of lower order modulators, each with its own quantizer. The quantizer input of each loop is fed to the next stage, where the quantization noise of the previous stage is corrected. At the final output, only the quantization error of the last stage exist, thus resulting in high order noise shaping. An digital error correction stage combines all quantizer outputs to produce the intended, oversampled digitized output. Integrator gain matching requirements between the error correction and cascaded modulators become a problem. In practical implementations, increasing the resolution of the multi-bit quantizer reduces the second-stage quantization error and increases the sensitivity to uncancelled quantization error from the first stage [5]. A cascaded, 4th order modulator with 5-bit quantization and a 6th order, 1-bit quantizer is described in sections 1.1 and 1.2 respectively.

1.1 4th order 5-bit Analog Modulator

The 4th order modulator shown in Figure 1 consists of two cascaded second order stages which include a 1-bit and 5-bit quantizer respectively. This will result in 4th order noise shaping with 5 bit quantization[3]. The error correction stage will combine the 1-bit digital output from the first stage with 5-bit and 1-bit digital outputs from the second stage, to yield an output comprised of the input signal plus a fourth order error term.
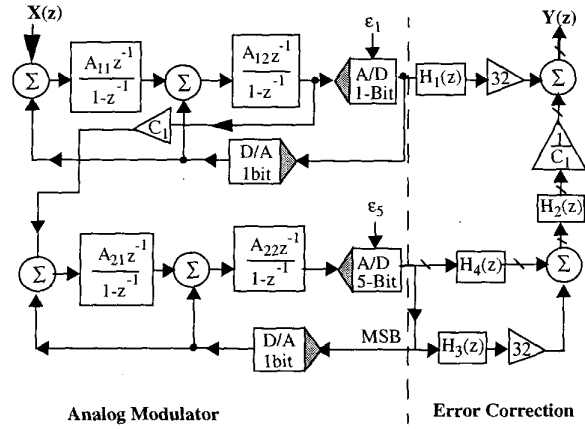

Analog Modulator   **Error Correction**

Figure 1: 4th Order Modulator

Transfer functions for the error correction filters of the 4th order system in Figure 1 can be given as follows:

$$H_1(z) = k(A_1 A_2)z^{-2}(1 - k(1 - z^{-1})^2) \qquad \text{Eq: 1}$$

$$H_2(z) = k(1 - z^{-1})^2 \qquad \text{Eq: 2}$$

$$H_3(z) = 1 - k(1 - z^{-1})^2 \qquad \text{Eq: 3}$$

$$H_4(z) = k(1 - z^{-1})^2 \qquad \text{Eq: 4}$$

$$k = \frac{1}{1 + (A_2 - 2)z^{-1} + (A_1 A_2 - A_2 + 1)z^{-2}} \qquad \text{Eq: 5}$$

The overall system transfer function Y(z) is below:

$$Y(z) = k^2 \left(X(z)(A_1 A_2)^2 z^{-4} + \frac{\varepsilon_5}{C_1}(1 - z^{-1})^4 \right) \qquad \text{Eq: 6}$$

Notice the 5-bit quantization noise error term, ε_5, with 4th order noise shaping $(1-z^{-1})^4$. This is the desired noise shaping required for this system transfer function. Following the error correction logic is a cascaded decimator section which includes a $Sinc^5$ filter and a 24 tap FIR filter[4].

1.2 6th order 1-bit Analog Modulator

The 6th order modulator consists of three cascaded second order stages as shown in Figure 2. This cascaded topology was chosen to take advantage of both the stability provided by its lower order sections and the 6th order noise shaping of the overall system. The 1-bit digital outputs of each of the three stages are combined and digitally filtered to yield an output comprised of the input signal plus a 6th order noise error term.
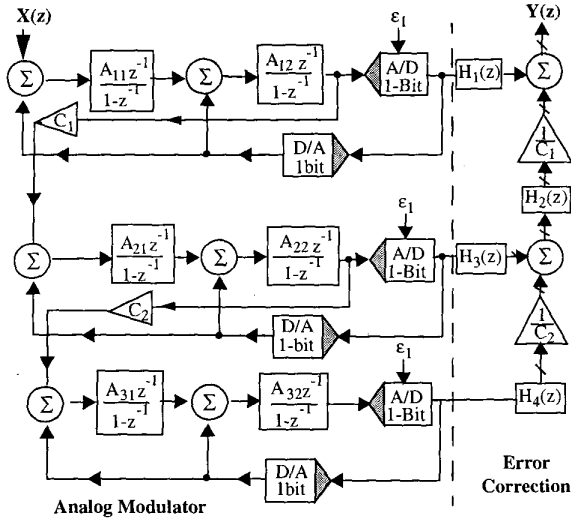

Figure 2: 6th Order Modulator

The 6th order modulator structure is very similar to the 4th order structure shown in Figure 1. Likewise, the error correction filters in the 6th order system have the same transfer functions as their counterparts in the 4th order system with the exception of $H_1(z)$ and $H_3(z)$, which are modified as follows:

$$H_1(z) = k^2(A_1A_2)^2 z^{-4}(1 - k(1 - z^{-1})^2) \quad \text{Eq: 7}$$

$$H_3(z) = kA_1A_2 z^{-2}(1 - k(1 - z^{-1})^2) \quad \text{Eq: 8}$$

The 6th order system transfer function for Y(z) is below:

$$Y(z) = k^3\left(X(z)(A_1A_2)^3 z^{-6} + \frac{\varepsilon_1}{C_1C_2}(1 - z^{-1})^6\right) \quad \text{Eq: 9}$$

Notice the desired 6th order noise shaping term for the 1 bit A/D quantization noise error, ε_1. Following the error correction logic is a cascaded decimator section which includes a Sinc[7] filter and a 24 tap FIR filter. Simulated ideal SNDR plots versus input amplitude for the ADC systems are shown in Figure 3.
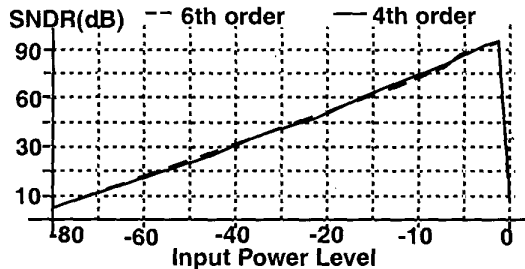

Figure 3: SNDR versus Amplitude Plots

2. Ideal Switch Capacitor Integrator

Switched capacitor $\Sigma\Delta$ analog modulators use discrete time integrators to perform the integration of signal error required for noise shaping. The ideal integrator analysis is and linear model response is described this section[5].

The three key circuit components of the discrete time integrators are the electrical switches, gain capacitors and the operational transconducance amplifier(OTA). An ideal switch capacitor integrator system is shown below:
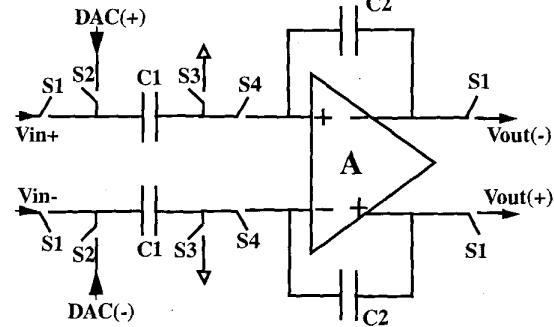

Figure 4: Switch Capacitor Ideal Integrator

The linear model used in Matlab simulation is shown in Figure 5 representing the switch capacitor discrete time system.
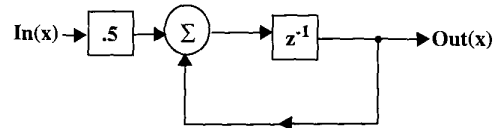

Figure 5: Ideal Integrator Model

The integrator transfer function in Equation 1 is represent by equation 10 and is shown below:

$$H_{Ideal}(z) = \frac{z^{-1}}{2(1 - z^{-1})} \quad \text{Eq: 10}$$

This z domain transfer function contains a pole exactly at the unit circle, simple zero at zero which is represented as a unit clock delay, and a dc gain term of a half[6].

3. Leaky Integrator Analysis

A discrete time integrator that contains a pole other than at the unit circle becomes an FIR filter rather than integrator. Passive parasitics around the circuit integrator and non ideal circuit parameters of the OTA also make the ideal transfer function non ideal. Hence, the name leaky integrator[7]. When we add the parasitics of wire capacitors to the common centroid layout, source

drain capacitors of the switches and input and output capacitances of the OTA, our integrator model is shown in Figure 6:
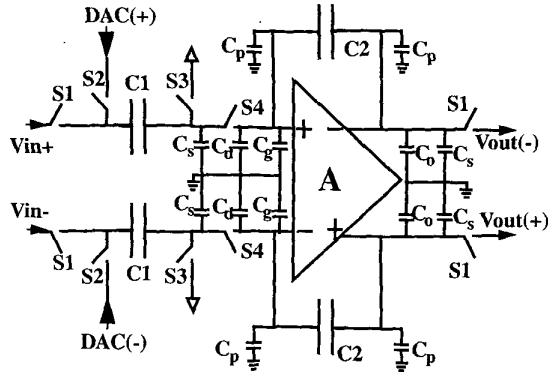

Figure 6: Switch Capacitor Leaky Integrator

Using conservation of charge derivations in the time domain, system variables gain eror (α), parasitic erors (η, γ), and offset error (ρ) can be derived as functions Cs, Cd, Cg, Cp, and Co. Also, S1 and S3 are out of phase clocks with respect to S2 and S4. These system variables for the leaky integrator are now shown below in Equations 11-14:

$$\eta = 1 + \frac{C_g + C_d}{C2(1+A)} \qquad \text{Eq: 11}$$

$$\gamma = \left(1 + \frac{(C1 + C_s + C_g + C_d)}{C2(1+A)}\right)^{-1} \qquad \text{Eq: 12}$$

$$\alpha = \frac{C1}{C2}\left(\frac{A}{1+A}\right) \qquad \text{Eq: 13}$$

$$\rho = \frac{C1}{C2}\left(\frac{A}{1+A}\right)\left(1 + \frac{C_s}{C1}\right) \qquad \text{Eq: 14}$$

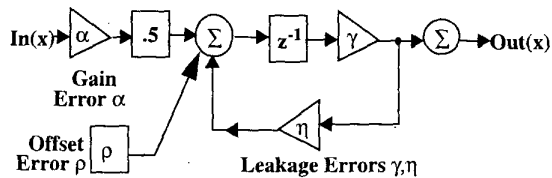The linear model for the Leaky Integrator is shown below:

Figure 7: Leaky Integrator Parasitic Model

$$H_{Leaky}(z) = \frac{\gamma z^{-1}(\alpha + 2\rho z)}{2(1 - \gamma\eta z^{-1})} \qquad \text{Eq: 15}$$

The γ and η feedforward and feedback parameters set the pole and zero of the switch capacitor integrator. Note η is > 1 and γ < 1. The α parameter is considered the gain error of the switch capacitor integrator[8,9]. The ρ parameter is analogous to a filtered dc offset. If this dc offset resides in the range of the OTA, it should not create a problem with respect to SNDR, only the input range. Thus, a sensitivity analysis with respect to the ρ parameter is not performed. In addition, all ADC gain parameters - namely A_{11} through A_{33}, C_1, C_2 - were set to 0.5 so that a unit capacitor based centroid capacitor layout could be used. Thus, the ratio of C2/C1 = 0.5. A folded cascode integrator with slew rate of 475 V/μs, Bandwidth of 1 Ghz and dc Gain of 58dB

was designed, For this layout, C2 = 2.64 pF, C1= 1.32 pF, Co= 8 pF, Cg = 3.2 pF, Cp = 0.01 pF, Cs = Cd = 0.4 pF. Thus, η = 1.00, γ = 0.99 and α = 0.5 and ρ = 0.65. These system parameters were simulated in Matlab for 4th and 6th order systems and results are below:
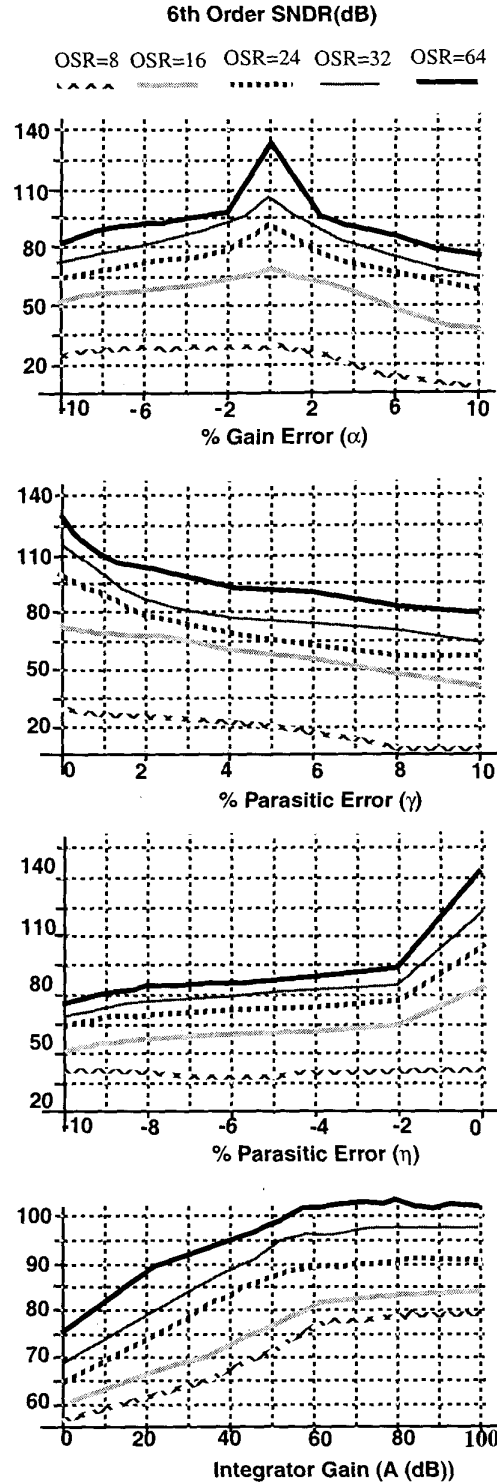

Figure 8: SNDR Sensitivity for 6th order

4. Evaluation Results

The table below show SNDR sensitivity with respect to system parameters for -6 dB and -12 dB attenuation in peak SNDR. Note values are entered as %.

4th Order SNDR(dB)

OSR=8　OSR=16　OSR=24　OSR=32　OSR=64

% Gain Error (α)

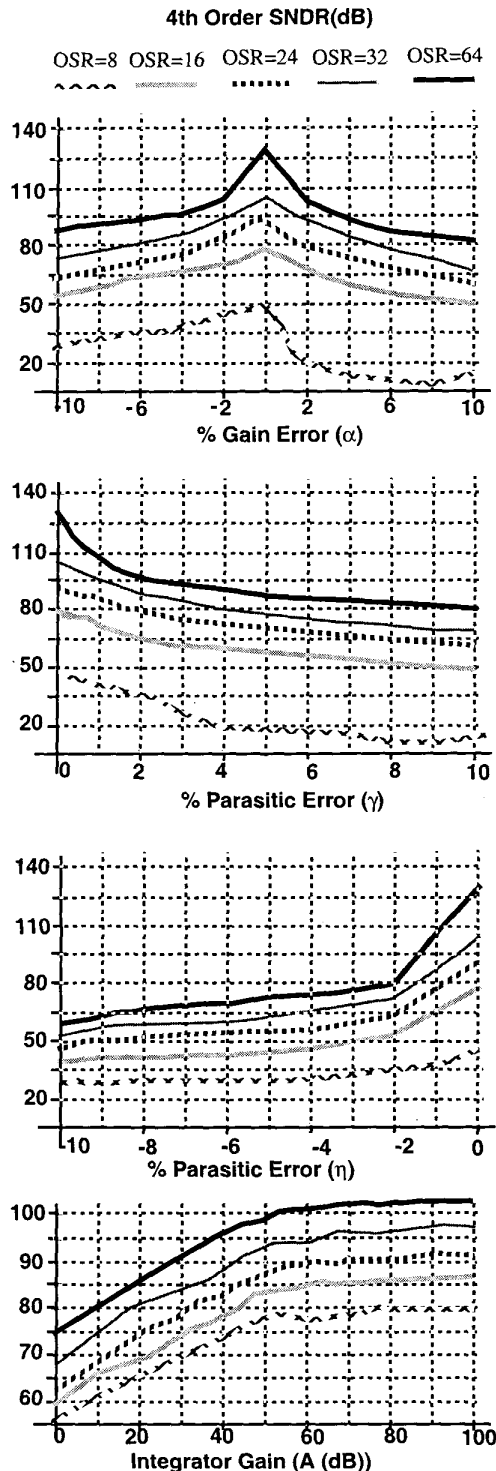% Parasitic Error (γ)

% Parasitic Error (η)

Integrator Gain (A (dB))

Figure 9: SNDR Sensitivity for 4th order

6th Order, 1-Bit	OSR				
System Parameters	8	16	24	32	64
% α (Gain Error)	3 | 6	2 | 4	1 | 4	1 | 4	.5|1.5
% γ (Parasitic Error)	4 | 6	3 | 5	1.3| 3	.7|1.5	.3 | .8
% η (Parasitic Error)	5|20+	1 | 2	.8 |1.6	.5 |1	.4 | 1
A (OTA dc Gain)	1 | 6	2 | 8	2 | 8	2 | 9	4 |10
4th Order, 5-Bit	**OSR**				
System Parameters	8	16	24	32	64
% α (Gain Error)	.1 | .4	1 | 2	.4 | 1	.3 | .9	.2| .7
% γ (Parasitic Error)	.4 | 1	.6 | 2	1.3| 3	1.4| 3	.4| 1
% η (Parasitic Error)	.4 | 1	.6 | .9	.6 | .9	.6 | .8	.2|.6
A (OTA dc Gain)	2 | 7	2 | 8	2 | 8	2 | 8	3 | 9

Table 1. -6dB | -12dB SNDR Sensitivity

5. Conclusion

In this paper we investigated the SNDR sensitivity phenomenon for a 6th order, 1-bit quantizer and a 4th order, 5-bit quantizer cascaded $\Sigma\Delta$ A/D system. Circuit parameters of the switched capacitor integrators such as amplifier open loop gain, integrator gain, and amplifier offsets and layout parasitics were quantified. Simulations data was presented and quantified to show % dependencies for that particular parameter.

6. References

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