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A 2GHz GaN Class-J Power Amplifier for Base Station Applications

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Abstract—The design and implementation of a high efficiency Class-J power amplifier (PA) for basestation applications is reported. A commercially available 10W GaN HEMT device was used, for which a large-signal model and an extrinsic parasitic model were available. Following Class-J theory, the needed harmonic terminations at the output of the transistor were defined and realised. Experimental results show good agreement with simulations verifying the class of operation. Efficiency above 70% is demonstrated with an output power of 39.7dBm at an input drive of 29dBm. High efficiency is sustained over a bandwidth of 140MHz.

Index Terms—Gallium compounds, high electron mobility transistors, power amplifiers.

I. INTRODUCTION

In modern communication systems there is an increasing demand for highly linear and efficient power amplifiers not only for portable devices but basestations as well. Large signal bandwidths that extend up to 20MHz and may soon reach 100MHz, together with high peak-to-average power ratios (PAPR) make the design of linear and highly efficient RFPAs for modern and future systems extremely challenging.

Currently, approaches to high efficiency amplification have gone down the path of harmonically tuned or switching PAs. Very promising results of Power Added Efficiency (PAE) above 70% have been reported for Class F/F^{-1} and Class E operation. These amplifiers' performance relies on a very specific impedance environment, limiting their bandwidth of operation and their resulting linearity is rather poor. For that reason they are commonly used under more complex transmitter systems like Envelope Tracking (ET) or Envelope Elimination and Restoration (EER).

Recently, a new class of operation was introduced by Cripps, termed as Class-J [1]. It requires a reactive second harmonic output termination which makes it suitable for GaN HEMTs. An output harmonic short, common in other classes of operation, is usually implemented using the device's output drain-source capacitance (C_{ds}). This is particularly hard to achieve in GaN HEMTs due to their substantially smaller C_{ds} .

Moreover, there is clearly the potential for highly efficient performance over wide-bandwidth. The exploitation of this class for wideband amplification with GaN HEMT

devices has been demonstrated in [2] and [3], using an active load-pulling system and waveform probing system to define the needed impedances. State-of-the-art efficiency of a Class-J was reported in [4], using a bare-die LDMOS and an optimized transistor model.

In this work, a Class-J PA design methodology was investigated, based on closed form equations for the acquisition of the needed impedances, a large-signal transistor model provided by the manufacturer and an estimation of the device's output parasitics. The models were used for simulations, impedance transformation and waveform de-embedding. Observing the de-embedded IV waveforms at the current generator plane verified the class of operation.

The amplifier was implemented using a 10W GaN HEMT device for a target frequency of 2.14GHz, on an RT/Duroid 5880 substrate. High maximum efficiency is demonstrated with good back-off performance, good linearity and substantial bandwidth. Experimental results are presented, plotted and discussed.

II. CLASS J THEORY AND OPERATION

The Class-J as introduced in [1], allows for significant second harmonic reactive output impedance. A complex impedance presented at the fundamental keeps the drain RF voltage above the "knee" region, avoiding the transconductance collapse and thus, highly non-linear behaviour.

In [5] it was noted that there exists a set of 2nd harmonic and fundamental impedance pairs that form a pool of impedances, the design space. All these cases deliver Class-B-like efficiency and output power, if biased as Class-B. The Class-J and J* represent limiting cases of this wider design space, while Class B is the middle case with a second harmonic short present.

Following analysis in [5], closed form equations for the design space have been derived and are given by (1) and (2), both normalized to the typical class A,B load-line resistance R_L and generalized by inclusion of the conduction angle. Each different case is denoted by d while α denotes the conduction angle.

Again, only fundamental and second harmonic terminations are considered in this theoretical formulation, as higher harmonics are assumed to be shorted by the output

drain-source capacitance. The effect of the third harmonic will be discussed in some detail later.

$$Z_{f_o} = \frac{\pi\sqrt{1+d^2}(1-\cos(\alpha/2))}{\alpha - \sin(\alpha)} \angle \phi \quad (1)$$

with $\phi = \text{atan}\left(-\frac{1}{d}\right) + \begin{cases} \pi/2, & \text{if } d \geq 0 \\ -\pi/2, & \text{if } d < 0 \end{cases}$

$$Z_{2f_o} = \frac{d}{2} \frac{\pi(1-\cos(\alpha/2))}{\sin(\alpha/2) - \frac{1}{3}\sin(3\alpha/2)} \angle -\pi/2. \quad (2)$$

So for Class-J operation with a device biased as Class-B ($d = 1, a = \pi$), (1) and (2) reduce to $Z_{f_o} = 1 + j$ and $Z_{2f_o} = -1.178j$. The expected current and voltage drain waveforms at the current generator plane for this particular case ($\alpha = \pi$), assuming a perfectly half-rectified sinusoidal drain current can be seen in Fig. 1. What should be noted is the large voltage swing, almost up to 3 times the supply voltage, caused by the presence of a strong second voltage harmonic that needs to be accommodated by the device.

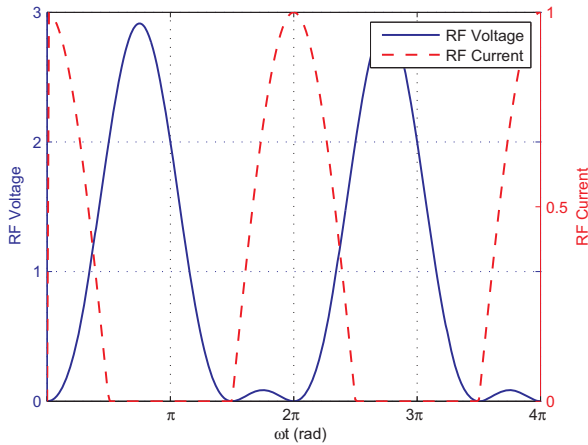


Fig. 1. Class J drain voltage and current normalized to DC components.

III. CLASS J DESIGN METHODOLOGY

The device used was CGH40010 by Cree, a 10W GaN HEMT, biased at very deep Class-AB with I_q about 5% of I_{max} . A V_{DS} of 28V was chosen, as it was the lowest valid drain-source voltage that can be applied to the large-signal transistor model. Moreover, it's low enough to allow for the high drain voltage swing of Class-J operation without exceeding the device breakdown voltage, given by the manufacturer as 84V.

After the biasing conditions were chosen the stability of the device was examined. The transistor was potentially unstable over a wide range of frequencies including the frequencies of interest, and therefore the use of a stabilisation network was inevitable. The amplifier was allowed to be conditionally unstable for particular input and output

impedances towards the outer of the Smith chart not to compromise on efficiency [6].

A. Input and output impedance terminations

The large-signal model was load pulled to determine the appropriate fundamental load-line resistance for the particular operating conditions. An $R_L = 36\Omega$ was chosen and (1) and (2) were de-normalized giving the needed impedances for Class-J operation. These calculated impedances refer to the current generator plane and had to be transformed to package plane impedances before proceeding to the matching network design.

For that reason, the model of the extrinsic parasitics and package parasitics was used, including a fixed C_{ds} capacitor. Observation of IV waveforms at the current generator plane in simulations was used to verify the class of operation. Although the drain-source capacitance in reality is non-linear, in GaN HEMTs it can be approximated as constant over V_{ds} as it does not change significantly and results indicate this is a valid assumption to make.

The inclusion of a non-linear C_{ds} would further increase the complexity of the extrinsic model, while giving higher precision on the shape of the de-embedded waveforms. Such an approach was not considered worthwhile as the results obtained were the expected. The input match was determined through source pulling and the output terminations had to be slightly tuned to account for the bilateral nature of the device.

B. Third Harmonic Output Termination

In classic Class-J theory, the 3rd harmonic output impedance is not taken into consideration as the current is assumed to be a perfectly half rectified sine-wave (no odd harmonics). In practice the efficiency and output power are expected to show some dependence on the 3rd harmonic impedance.

This was investigated in simulations by sweeping the 3rd harmonic output impedance at the package plane, for fixed input power while plotting PAE and output power. The results show some favourable impedance as can be seen in Fig. 2 due to the variable power dissipation at the 3rd harmonic.

C. Matching Network Design And Layout

With known targets for input and output impedances the matching networks were designed using a fully distributed architecture, except for the input and output decoupling capacitors, the stabilisation network and a number of DC bias injection bypass capacitors. Harmonic control up to the 2nd input and 3rd output harmonics was employed by the matching networks.

The networks were implemented on RT/Duroid 5880 substrate, with $E_r = 2.2$ and thickness of 0.787mm. The schematic can be seen in Fig. 3. Due to the low dielectric constant the transmission lines were longer and

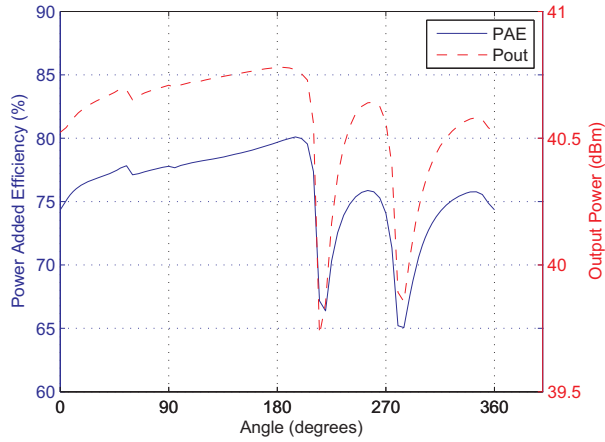


Fig. 2. Third output harmonic reflection coefficient angle sweep showing dependence of output power and PAE.

thus introduce higher losses, but the design was made less prone to fabrication errors. After electromagnetic (EM) simulations, the input and output matching networks were fine tuned to account for losses and EM coupling effects.

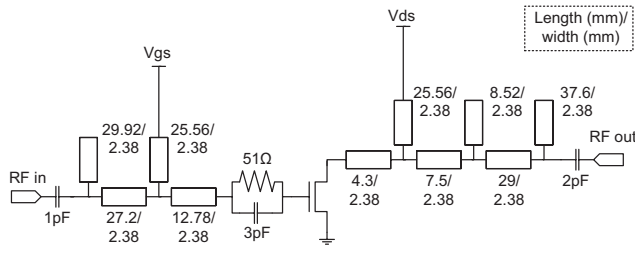


Fig. 3. Simplified amplifier schematic.

D. Simulation Results

Using the device model and the results from the EM simulation of the matching networks, the overall schematic was simulated and the expected performance of the PA can be seen in Fig. 4. A maximum PAE of about 73% is predicted under 3.5dB of gain compression, delivering just above 40dBm of output power. The efficiency remains at relatively high levels with PAE between 50-60%, even for 5-6dB back-off from the peak efficiency point.

Fig. 5 illustrates the simulated voltage and current drain waveforms at the current generator plane. The voltage peaks close to 84V as expected. At that point a current “hump” can be observed which can be accounted to the high voltage swing and has been observed elsewhere for a Class F^{-1} [7].

IV. EXPERIMENTAL RESULTS

The input and output matching networks were implemented on RT/Duroid 5880 substrate as two separate

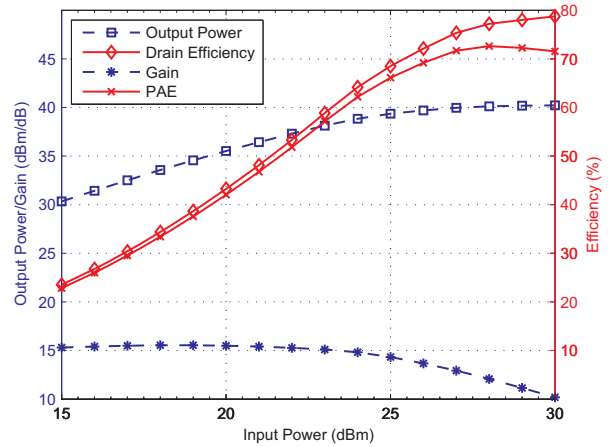


Fig. 4. Input power sweep showing the expected output power, gain and efficiency of the Class-J at 2.14GHz.

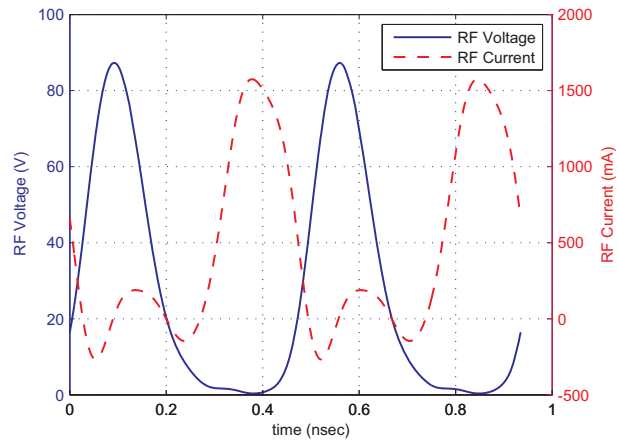


Fig. 5. Simulated Class-J drain voltage and current at the current generator plane.

boards and mounted directly on the heat sink. The PA can be seen in Fig. 6 measuring a board size of 13.5cm x 6.5cm. The size can be reduced by choosing a different substrate. Good agreement between simulations and measurements was achieved, especially considering the high board losses that cannot be accurately modelled in simulations.

The measured performance under continuous wave input is shown in Fig. 7 for a frequency of 2.13GHz. The discrepancy in frequency (less than 0.5%) can be accounted to the model used or errors in the fabrication of the PCBs. The PA achieves a maximum PAE of 64.5% at an input drive of 29dBm into 3.3dB of gain saturation, delivering an output power of 39.75dBm. For a 5dB back-off from the maximum PAE point the PA still operates with above 50% efficiency.

The input signal’s frequency was swept over a 200MHz bandwidth from 2.04 to 2.24GHz for a constant input

drive of 29dBm. For most of the bandwidth the amplifier's efficiency stays well above 50%. For 140MHz bandwidth between 2.08-2.2GHz the output power stays above 39dBm and the efficiency over 60%. Although wideband operation was not a design target, the substantial bandwidth achieved indicates the potential of Class-J.

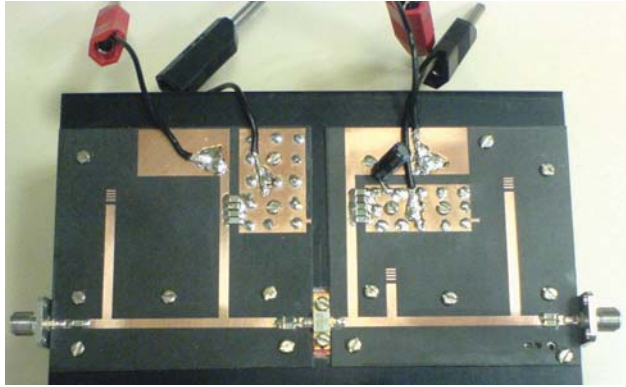


Fig. 6. Photograph of the implemented PA.

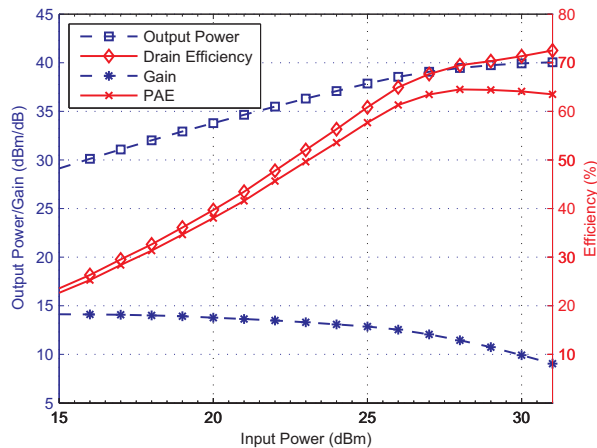


Fig. 7. Measured Class J performance over input power at 2.13GHz.

V. CONCLUSION

In this paper, the design of a high-efficiency Class-J power amplifier has been reported using a packaged 10W GaN HEMT. The use of a harmonic balance simulator, together with a large-signal model and an extrinsic parasitic components model including a fixed drain-source capacitance C_{ds} was proven sufficient for the design of a Class-J PA. Waveform de-embedding has been used in simulations in order to verify the class of operation. The amplifier shows a maximum PAE of 64.5% at 2.13GHz with an output power of 39.7dBm and a power gain of 10.7dB at the maximum point. Performance further away from the maximum PAE point is still high and stays above

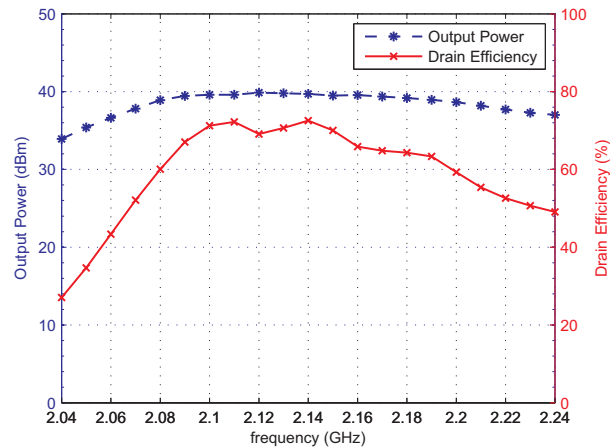


Fig. 8. Measured Class J performance over 200MHz of bandwidth for an input power of 29dBm.

50% for 5dB back-off. Moreover, efficiency is maintained over a bandwidth of 140MHz.

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