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Current Sharing of Parallel SiC MOSFETs under Short Circuit Conditions

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Abstract
Device-to-device parametric variations (e.g. threshold voltage $V_{TH}$, gate resistance $R_G$ and junction temperature $T_J$) can cause variations in the short-circuit currents conducted through parallel-connected devices. In this paper, the impact of variations in $V_{TH}$, $R_G$ and $T_J$ on current sharing under short-circuits is investigated using measurements and electrothermal modelling.

Introduction
In this paper, the performance of parallel SiC MOSFETs under short circuit conditions is investigated. SiC modules comprise of power MOSFETs connected in parallel for current sharing. Under ideal conditions, these devices should share short circuit currents equally. However, parametric differences between parallel connected devices, (e.g. threshold voltage $V_{TH}$, gate resistance $R_G$ and junction temperature $T_J$) can cause variations in the short circuit currents conducted through each device [1-4]. Even when devices are initially matched, phenomena like differential $V_{TH}$ drift from different rates of charge trapping of parallel connected SiC MOSFETs can cause small differences in $V_{TH}$ over the operational life of the device. In this paper, the impact of variations in $V_{TH}$, $R_G$ and $T_J$ between parallel connected SiC MOSFETs on current sharing under short circuit conditions is investigated. An electrothermal model that can accurately predict the short circuit current mismatch as a function of junction temperature difference and threshold voltage difference has been developed. By extending the model to more parallel devices, design guidelines for parallel connection of SiC MOSFETs are provided.

Experimental Set-up and Measurements
The circuit diagram of the experimental set-up for the short circuit measurements is shown in Fig. 1(a) while a picture of the test rig is shown in Fig. 1(b). The circuit comprises of a DC voltage source, a 90 µF DC link capacitor, a control 1.7kV/1000A silicon IGBT module with datasheet reference FF1000R17IE4 and the devices-under-test (DUTs). The current through the parallel devices is measured using a Rogowski coil from Powertek. The current and voltage waveforms are captured using an oscilloscope from Teledyne LeCroy.

The DUTs are 1.2kV/20A SiC MOSFETs from STmicroelectronics with datasheet reference SCT20N120 and 1.7kV/5A SiC MOSFETs from Cree with datasheet reference C2M1000170. Fig. 2(a) shows the measured short circuit current measured with different gate-source voltages ($V_{GS}$). As expected, the peak short circuit current and short circuit energy increases with reduced $V_{GS}$ due to higher channel resistance. Fig. 2(b) shows short circuit measurements with different $R_G$ where it can be seen that there is a marginal increase in the peak short circuit current as $R_G$ is reduced.
Fig. 2(a). Measured short circuit currents in the SiC MOSFETs with different $V_{GS}$.

Fig. 2(b). Measured short circuit currents in the SiC MOSFETs with different $R_G$.

As the gate resistance is increased from 68 $\Omega$ to 100 $\Omega$ and 120 $\Omega$, the short circuit energy decreases from 0.364 J to 0.363 J and 0.362 J respectively.

Short circuit measurements have been performed on SiC MOSFETs with different threshold voltages. As expected, the device with the lower threshold voltage conducts a higher short circuit current due to reduced channel resistance. The ON-state resistance of the MOSFET can be expressed by the equation below, where the first term accounts for channel resistance while the 2nd term accounts for the drift resistance. The presence of the $V_{TH}$ parameter in the denominator results in increased short circuit current as $V_{TH}$ is reduced.

$$R_{DSON} = \frac{i_{ch}}{W\mu COX(V_{GS}-V_{TH})} + \frac{i_{drift}}{q\mu N DA}$$

(1)

Fig. 3(a) shows the results for parallel connected SiC MOSFETs with 20% variation in threshold voltage with $V_{GS}$ set to 15 V while Fig. 3(b) shows similar measurements with $V_{GS}$ set to 17 V. The measured short circuit energy difference between the parallel MOSFETs is 5.1% at $V_{GS}=15$ V and 8.1% at $V_{GS}=17$ V.

Fig. 3(a). Measured Short circuit current for parallel 1.2kV/20A SiC MOSFETs with 20% difference in $V_{TH}$ and $V_{GS}$=15 V

Fig. 3(b). Measured Short circuit current for parallel 1.2kV/20A SiC MOSFETs with 20% difference in $V_{TH}$ and $V_{GS}$=17 V

It is expected that $V_{TH}$ difference becomes less important as the voltage rating of the devices increase, since channel resistance becomes dominated by the drift resistance i.e. the 2nd term in Equation (1) dominates the first term. Fig. 4(a) shows short-circuit measurements on parallel 1.7kV/5A SiC MOSFETs with 11.1% difference in $V_{TH}$ while Fig. 4(b) shows similar measurements with 125°C difference in initial junction temperature. For the 1.7kV MOSFETs, an 11.1% difference in $V_{TH}$ between parallel devices results in a 5.5% difference in short circuit energy while a 500% difference in $T_J$ results in a 9.98% difference in short circuit energy. These results presented correspond to different voltage rated devices from different manufacturers. Further results on more devices will give a fuller representation on how $V_{TH}$ mismatch impacts different voltage ratings.
Measurements have also been performed on parallel 1.2kV SiC MOSFETs with different gate resistance. Fig. 5(a) shows measurements with a 20\% difference in $R_G$ while Fig. 5(b) shows measurements with over 300\% difference in $R_G$. In Fig. 5(a), the difference in short circuit energy is 4.02\% while in Fig. 5(b) it is 5.35\% with the faster switching device dissipating more short circuit power in both cases. Differences in gate resistance do not contribute to significant variation in short circuit energy in the parallel pair if the differences in $R_G$ do not exceed 50\%. This is because the short circuit duration is much longer than the switching time constant of the devices, which is estimated to be 20 ns.

Measurements have also been performed on parallel SiC MOSFETs with different initial junction temperatures. Fig. 6(a) shows measurements on parallel devices with a junction temperature difference set at 25 °C while Fig. 6(b) shows similar measurements with the junction temperature difference set at 125 °C.

In both cases, the device with the lower initial junction temperature conducts a higher short circuit current. The short circuit energy in the device with $T_J$ set to 25 °C is 0.301 J while that of the device with $T_J$ set 50 °C and 150 °C is 0.283 J and 0.268 J respectively. The positive temperature coefficient of the ON-state resistance means that the
device with the initially higher junction temperature will conduct a smaller short circuit current. However, as the device voltage rating increases, it is expected that the difference in short circuit energy between the parallel pair will increase for the same variation in junction temperature.

### Electrothermal Modelling of Short Circuits

In this section, an electrothermal model for parallel devices in short circuits is introduced and used to predict the short circuit performance of parallel connected SiC MOSFETs. The static and dynamic characteristics of the model are first developed so that there is good matching between the model and experimental measurements. The static characteristics of the SiC MOSFETs are modelled using fitted exponential equations for $I_{DS}$ as a function of the overdrive voltage $(V_{GS} - V_{TH})$ and temperature $T_J$. The equation below shows the relationship between $I_{DS}$ and $V_{DS}$, where the constants $a$ and $b$ are extracted from curve fitting and vary according to the over-drive voltage $(V_{GS} - V_{TH})$ applied to the device using interpolation.

$$I_{DS} = -a \cdot e^{b \cdot V_{DS}} + a$$

The model has been made temperature dependent by fitting the values of the constants $a$ and $b$ at 25°C and 200°C. Using biharmonic (V4) interpolation, the simulation produces output values of $a$ and $b$ as functions of both $(V_{GS} - V_{TH})$ and $T_J$. Using this fitting method, the on-state resistance of the device is calculated as the division between $V_{DS}$ and $I_{DS}$ as detailed in the following equation.

$$R_{dson} = \frac{V_{DS}}{-a \cdot e^{b \cdot V_{DS}} + a}$$

Using datasheet parameters and characteristics, the electrothermal model has been parameterized. The temperature dependency of the ON-state resistances and threshold voltage have been accounted for along with the non-linear inter-terminal capacitances. Fig. 7(a) shows the matched output characteristics between the model and the datasheet while Fig. 7(b) shows matched gate transfer characteristics.

To check the accuracy of the models, the results of the simulations have been plotted together with the measurements. Fig. 8(a) shows the simulated and measured short circuit current while Fig. 8(b) shows the measured and simulated drain-source voltage across the device. In Fig. 8(b), the negative spike during the start of the short circuit is due to the voltage drop across the drain inductance during current rise while the positive spike at the end of the short circuit is due to the voltage across the drain inductance during current fall. The simulated $V_{DS}$ shows more oscillation than what is measured because of more temperature dependent resistive damping in the measurements.

Short circuit characteristics have also been modelled and matched with the experimental measurements presented in Fig. 9 for parallel connected MOSFETs with different threshold voltages and initial junction temperatures. Fig. 9(a) shows the short circuit simulations and experimental measurements for parallel devices with different $V_{TH}$ while Fig. 9(b) shows a similar plot for parallel devices with different initial junction temperatures. Comparing these modeled short circuit characteristics to the measurements in Fig. 3 and Fig. 6 for the 1.2kV devices, it can be seen that the short circuit behavior of the MOSFET is captured. When the difference
between the parallel devices is in $V_{TH}$, there is convergence in the short circuit current whereas when it is in junction temperature, there is no convergence. This is apparent both in the measurements and simulations. In the final paper, the model is used to provide design guidelines for paralleling. By increasing the number of parallel devices and adding more variation between electrothermal parameters, the impact of electro-thermal variation on short circuit robustness is further investigated.

**Fig. 8(a)** A comparison between simulated and measured short circuit currents in the 1.2kV SiC MOSFET

**Fig. 8(b)** A comparison between simulated and measured short circuit Drain-source voltage in the 1.2kV SiC MOSFET

**Fig. 9(a)** Simulated Short circuit characteristics for parallel SiC MOSFETs with 20% variation in $V_{TH}$.

**Fig. 9(b)** Simulated Short circuit characteristics for parallel SiC MOSFETs with 100% variation in $T_j$.

**Conclusion**

In this paper, the impact of variation in threshold voltage ($V_{TH}$), gate resistance ($R_G$) and junction temperature ($T_j$) between parallel SiC MOSFETs on short circuit robustness has been studied. It is shown that the most critical parameter is $V_{TH}$, followed by $T_j$ and $R_G$. Electro-thermal modelling is required for further investigation of how these parameters affect short circuit performance of parallel devices. In the extended paper, the role of drain inductance on the DC link voltage and short circuit current is explored using electrothermal modelling and further measurements. Using the electrothermal model, design guidelines are provided for maximizing short circuit robustness of parallel devices.

**References**


