Investigating the Reliability of SiC MOSFET Body Diodes using Fourier Series Modelling

R. Bonyadi, O. Alatise, S. Jahdi, J. Hu, L. Evans, P. A. Mawby
School of Engineering
University of Warwick
Coventry, UK
r.bonyadi@warwick.ac.uk, o.alatise@warwick.ac.uk, s.jahdi@warwick.ac.uk,
ji.hu@warwick.ac.uk, p.a.mawby@warwick.ac.uk, levans1@jaguarlandrover.com

***Abstract*— Using the Fourier series solution to the ambipolar diffusion equation, the robustness of the body diodes of SiC MOSFETs during reverse recovery has been studied. Parasitic bipolar latch-up during the reverse recovery of the body diode is a possible if there is sufficient base current and voltage drop across the body resistance to forward bias the parasitic BJT. SiC MOSFETs have very low carrier lifetime and thin epitaxial drift layers, which means that the dV/dt during the recovery of the body diode can be quite high. This dV/dt coupled with the parasitic drain-to-body capacitance can cause a body current. The paper introduces a new way of assessing the reliability of SiC MOSFETs during the reverse recovery of the body diode. The impact of switching rates, parasitic inductances and carrier lifetime on the activation of the parasitic BJT has been studied.**

***Index Terms*—Ambipolar Diffusion Equation, Fourier series, MOSFET, PiN Diodes, Body Diode, Inverter.**

I. INTRODUCTION

Power MOSFET circuits often use PiN body diodes as the anti-parallel diodes. This includes applications such as DC-DC buck converters, bridge topology switching circuits, high performance PV converter cell and can also be employed in synchronous rectified BLDC motor drive inverter circuits [1-4]. The voltage blocking drift region sandwiched between the drain and source shapes the PiN body diode in a vertical MOSFET. A significant portion of electrical stress and power losses in these applications are caused by the diode snappiness, high *dV/dt* across the body diode and high reverse recovery charge of the body diode [5]. The large reverse recovery is the result of high excessive amount of carriers stored in the charge storage region (drift layer) of the diode. The lifetime control techniques (gold or platinum doping as well as irradiation) are not applicable to reduce the carrier lifetime in some devices such as CoolMOS. The robustness of the MOSFET body diode is the main concern especially under hard commutation of the device. This is the case in applications like synchronous rectification, or motor drives or primary side switching of SMPS power supplies circuits [6]. High demands for higher frequency and more efficient converters introduced wide bandgap materials such as SiC material and consequently high blocking voltage SiC MOSFETs were developed. Carrier lifetime in of SiC material, with the same base doping as silicon material, is much shorter. SiC device can withstand higher reverse voltages and consequently 10 times smaller thickness is needed to have the same level of voltage blocking capability as silicon-based devices [7]. Thus, SiC MOSFETs show smaller reverse recovery with a higher breakdown voltage. The effect of using SiC MOSFET in synchronous rectification is studied in [2] which shows a negligible SiC MOSFET body diode reverse recovery and in addition to that, it showed feasibility of increasing the switching frequency. All in all, SiC devices are a suitable candidate for power application named above due to their superior performance. However, there are concerns regarding the reliability of SiC MOSFET body diode.

Vertical MOSFET structure consists of a parasitic NPN BJT coupled with a PiN body diode. The parasitic BJT can switch-on if the emitter-base voltage is forward biased, the base-collector voltage is reverse biased and there is sufficient body current in the base of the BJT. When the body current rises the voltage drop in the base of the BJT due to existence of body resistance increases. Body resistance is highly dependent to the doping and temperature of the P-body. If the voltage drop becomes greater than the base-emitter voltage, then the parasitic BJT latches-up. This can happen at high temperatures. By grounding the source to the body using a high dose body implant and a common metal contact, the parasitic BJT is prevented from latching. Moreover, the high voltage variation (*dV/dt*) of the body diode during reverse recovery coupled with the parasitic drain-to-body capacitance within the MOSFET can produce enough amount of body current ($C \cdot dV/dt$) swich the parasitic BJT on. This phenomenon happens especially in SiC MOSFETs where *dV/dt* is high, minority carrier lifetime in the drift region is very short and the body diode is snappy. In this paper, the reliability of the SiC MOSFET body diode under reverse recovery is investigated experimentally and by modelling. The body diode of the MOSFET has been modelled using the Fourier series solution to the ambipolar diffusion equation [8]. The impact of the switching rate, carrier lifetime and

EPSRC project in collaboration with Jaguar Land Rover PLC and the University of Warwick

circuit parameters on the diode recovery characteristics is investigated by the model and compared with experimental measurements. Section II describes the development of the model for the body diode, section III describes the experimental measurements and model validation, section IV discusses the results while section V concludes the paper.

.

II. Body Diode Model Development

The following model uses the Fourier series to reconstruct the ADE in the drift region to explain the electron and holes behaviour in the plasma region. The ADE is a 2nd order partial differential equation describing the minority carrier distribution profile in the drift region of bipolar devices as a function of space and time. The boundary conditions for the solution are set by the PN- and N-N+ junctions of the body diode. Reconstruction of ADE using Fourier series is the most computationally inexpensive solution to achieve the plasma behaviour of the device [9-18]. Drift layer conductivity modulation is the phenomenon through which low conduction losses are enabled in PiN diodes and depends on minority carrier injection into the drift region. If the number of injected holes to the drift region becomes much greater than the background doping of the drift region, charge neutrality requires that the concentration of electrons and holes be equal to each other in that region: $p(x) = n(x)$. Using the continuity equations for the electrons and holes and the charge neutrality equation, the ADE is resulted [19]:

$$\frac{\partial p(x,t)}{\partial t} = -\frac{p(x,t)}{\tau_{HL}} + \left(\frac{2\mu_n\mu_p V_T}{\mu_n+\mu_p}\right)\frac{\partial^2 p(x,t)}{\partial x^2} \quad (1)$$

where, τ_{HL} is the high level lifetime [12] in the drift region. Diffusivity in ADE is calculated using the Einstein relationship ($D = \frac{kT}{q}\mu$) as below and D_n and D_p are the diffusion coefficients for electron and holes respectively:

$$D = \frac{2\mu_n\mu_p V_T}{\mu_n+\mu_p} = \frac{2D_nD_p}{D_n+D_p} \quad (2)$$

The Ambipolar Diffusion Length is the length is $L_a = \sqrt{D\tau_{HL}}$. ADE is reconstructed using Fourier series in one dimension. Each term of the ADE in equation (1) is multiplied in cos $(\frac{\pi k(x-x_1)}{x_2-x_1})$ and then integrated with respect to x_1 and x_2 which determine the start and ending points of the depletion regions in the drift region from P side and N^- side respectively [11, 20]:

$$Term\ 1 = \int_{x_1}^{x_2}\frac{\partial p(x,t)}{\partial t}\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right)dx = \sum_{\substack{n=1\\n\neq k}}^{\infty}\frac{n^2p_n}{n^2-k^2}\left[\frac{dx_1}{dt} - (-1)^{n+k}\frac{dx_2}{dt}\right] + \frac{x_2-x_1}{2}\frac{dp_k}{dt} + \frac{p_k}{4}\left[\frac{dx_1}{dt} - \frac{dx_2}{dt}\right] \quad (3)$$

$$Term\ 2 = \int_{x_1}^{x_2}\frac{p(x,t)}{\tau_{HL}}\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right)dx = \frac{x_2-x_1}{2}p_k(t) \quad (4)$$

$$Term\ 3 = D\int_{x_1}^{x_2}\frac{\partial^2 p(x,t)}{\partial x^2}\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right)dx = D\left[\frac{\partial p(x,t)}{\partial x}\Big|_{x_2}(-1)^k - \frac{\partial p(x,t)}{\partial x}\Big|_{x_1}\right] - D\left(\frac{\pi k}{x_2-x_1}\right)^2\frac{x_2-x_1}{2}p_k(t) \quad (5)$$

where $p_k(t)$ are the Fourier series coefficients. Putting these three terms in ADE (equation 1) gives the reconstruction of the ADE using Fourier series [10, 21]. In the equation below, *k=0* is the DC-term of the ADE and *k>0* shows the rest of the harmonic terms of the Fourier series. The higher k is, the more accurate the reconstruction will be:

$$p(x,t) = \sum_{k=0}^{\infty}p_k(t)cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right) \quad (6)$$

$k > 0$:

$$\frac{dp_k}{dt} = \frac{2D}{x_2-x_1}\left[\frac{\partial p}{\partial x}\Big|_{x_2}(-1)^k - \frac{\partial p}{\partial x}\Big|_{x_1}\right] - p_k\left(\frac{1}{\tau_{HL}} + \frac{D\pi^2k^2}{(x_2-x_1)^2}\right) - \frac{2}{(x_2-x_1)}\left(\sum_{\substack{n=1\\n\neq k}}^{\infty}\frac{n^2p_n}{n^2-k^2}\frac{dx_1}{dt} - (-1)^{n+k}\frac{dx_2}{dt}\right) - \frac{p_k}{2(x_2-x_1)}\left(\frac{dx_1}{dt} - \frac{dx_2}{dt}\right)$$

$k = 0$:

$$\frac{dp_0}{dt} = \frac{D}{x_2-x_1}\left[\frac{\partial p}{\partial x}\Big|_{x_2} - \frac{\partial p}{\partial x}\Big|_{x_1}\right] - \frac{p_0}{\tau_{HL}} - \frac{1}{(x_2-x_1)}\sum_{n=1}^{\infty}p_n\left(\frac{dx_1}{dt} - (-1)^n\frac{dx_2}{dt}\right)$$

III. Model Validation

Validation of the PiN diode device model using the Fourier series ADE reconstruction (F.S ADE) is carried out by comparing the result of the simulation with a finite element device modelling simulator (Silvaci) and with the experiments. A 1200V/45A IXYS PiN diode (DSI45-12a) coupled with a 1200V/38A IXYS IGBT (IXDH20N120D1) was tested under clamped inductive switching conditions using the double pulse test method. Next, the reverse recovery characteristic of the body diode of a SiC MOSFET from Cree (C2M0160120D) is modelled and validated by experimental measurements. The circuit arrangement comprised of the high side free-wheeling PiN diode, an inductor for current commutation, a high voltage power supply, a gate drive circuit and a low side switch. In order to capture the reverse recovery waveform of the body diode of the SiC MOSFET, the high side MOSFET of the half-bridge is clamped (gate is connected to the source) and the MOSFET acts as a free-wheeling diode in the circuit. The low side IGBT/MOSFET is initially switched on to charge the inductor, then it is switched off so that the current free-wheels in the PiN diode. When the IGBT is switched on again, current commutates from the free-wheeling diode into the low side IGBT/MOSFET. The low side MOSFET gate and drain-source voltage and current waveforms along with the diode voltage (V_{AK}) were captured using a Tektronix oscilloscope. Devices under test (DUT) were placed in a thermal chamber to keep the temperature constant at desired temperatures. The current slope (*dI/dt*) was varied by the gate resistance of the low side switch. The comparison of the diode turn-off current from the experimental measurements, the F.S ADE model and a finite element simulation from Silvaco is shown if Fig. 1. To obtain an accurate matching between the results, the datasheet parameters alongside with the known material properties of devices were used in both

simulation platforms. Devices physical parameters were adjusted for fine matching and calibration of the F.S.ADE and Silvaco simulations.

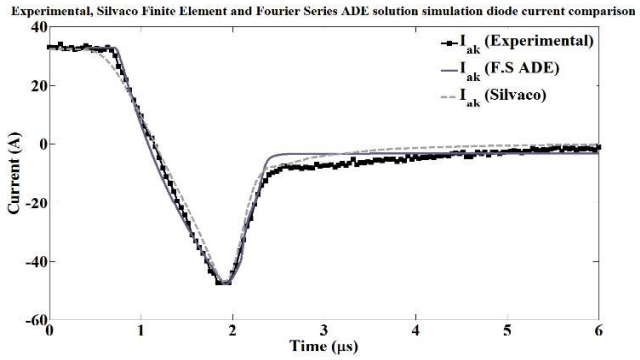


Fig. 1. Simulation validation: Diode reverse recovery current waveform from the experimental results, Silvaco Finite Element device simulation and Fourier Series ADE reconstruction simulation at the room temperature using 22 Ω gate resistance.

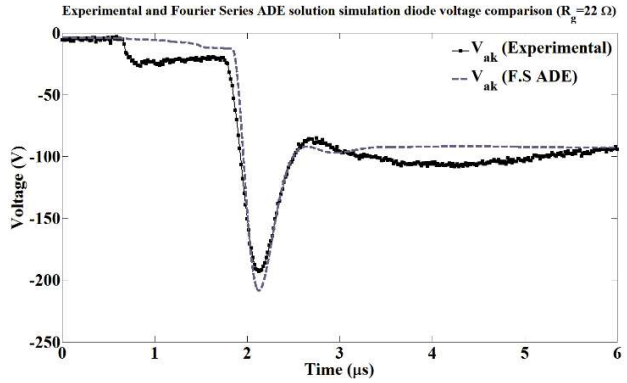


Fig.2. Simulation validation: Diode reverse recovery voltage waveform from the experimental results and Fourier Series ADE reconstruction simulation at the room temperature using 22 Ω gate resistance.

Fig. 2 illustrates the comparison between the diode voltage during the turn-off using the F.S ADE solution and the experiments. The parasitic inductances in the model have been varied between 10 to 100 nH to match the experimental measurements. The time displacement between the peak voltage overshoot and the peak reverse recovery current is critical for accurate determination of the switching energy especially since they both depend on the switching rate. The peak reverse recovery current occurs very shortly after the diode voltage starts to rise.

Measurement of the diode turn-off current switched at different rates have been compared with the model. The results are shown in Fig. 4 for four different switching rates. Both the measurements and simulation show that the peak reverse current increases with the switching rate. The reduction in *dI/dt* and the increase in the peak reverse current have been correctly predicted by the model.

Matching of the F.S ADE with the experimental results from the Cree SiC MOSFET body diode is illustrated in Fig. 4. The result indicates a very good correlation between simulation and the experiments.

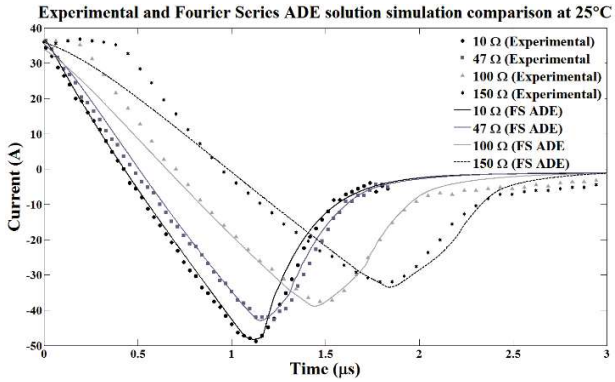


Fig. 3. PiN diode reverse recovery waveform for different IGBT gate resistances (different dI/dt) - Comparison between the experimental results and the simulation results using the Fourier Series ADE reconstruction.

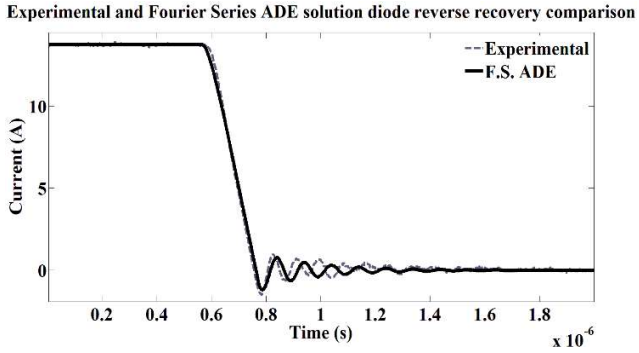
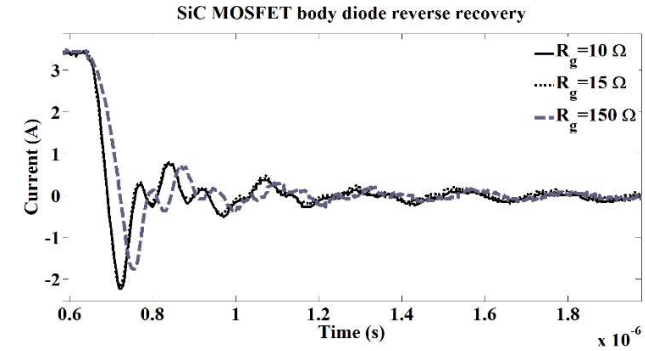


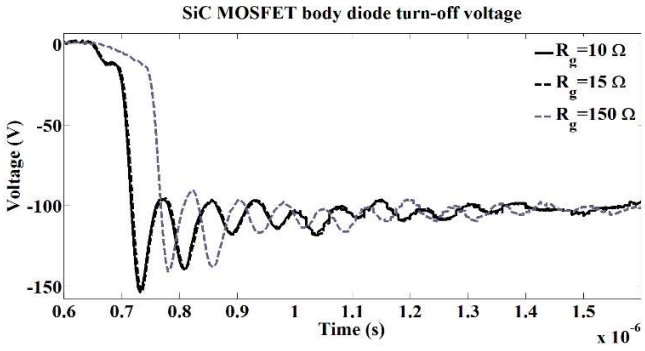
Fig. 4. SiC MOSFET body diode reverse recovery waveform – Comparison between the experimental results and the simulation using the Fourier series ADE reconstruction.

IV. Results and Discussion

The body diode measurements were designed to test the SiC MOSFET at two different initial currents (3.4 A and 13.4 A) and the switching rate of the devices were varied by the gate resistance at room temperature. The DC supply voltage was set to be 100 V. At 13.4A forward current, the devices failed at large switching rates (*dI/dt*) which was due to hard current commutation. At the same high switching rate devices survived under 3.4A forward current. At 13.4A forward current devices were able to withstand the reverse recovery process under smaller *dI/dt* and the waveforms were captured from the test rig. Fig. 5 illustrates the switching transient current and voltage waveform of SiC MOSFET body diode at 3.4A using different gate resistances while Fig. 6 shows the same result at higher forward current of 13.4A. As demonstrated previously in silicon devices, the *dI/dt* of the reverse recovery can be reduced significantly by changing the gate resistance.



(a)

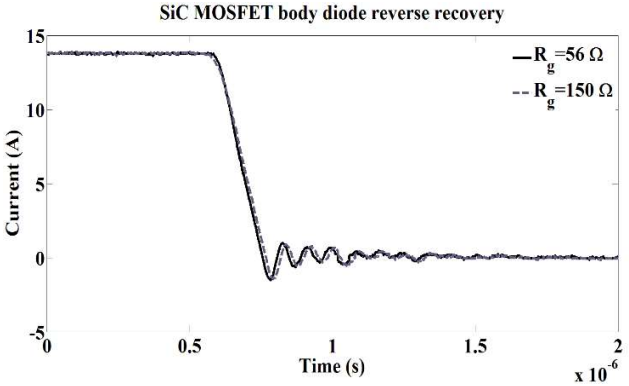


(b)

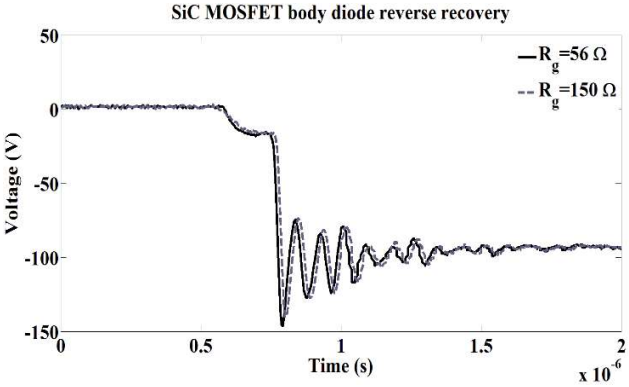
Fig. 5 SiC MOSFET body diode reverse recovery waveform for different switching rates with a forward current of 3 A (a). SiC MOSFET body diode voltage waveform for different switching rates with a forward current of 3 A (b)

In silicon-based devices, varying the gate resistance has a significant impact on the switching rate of the devices and *dI/dt* can be reduced by using a larger gate resistance. However, the experiments show that this is not the case for SiC MOSFET body diode.At small gate resistances slight changes in the gate resistance (i.e. using 15Ω instead of 5Ω) does not make a huge variation in the result and it stays almost identical. Only at much lower *dI/dt* obtained by using 150Ω can the changes be observed. As expected by significantly increasing the gate resistance, the slope of the reverse recovery decreases and the peak voltage and current decreases. The parasitic inductances in the test rig coupled with the much faster switching rate of the SiC devices induce the oscillations observed in the current and voltage. Using the F.S ADE model developed, the impact of varying the MOSFET gate resistance, emitter inductance, carrier lifetime in the drift layer and the thickness of the drift region is investigated on the behaviour of the SiC MOSFET body diode under reverse recovery are investigated. As expected and shown in Fig. 7(a) changing the gate resistance slightly decreases the peak current of the reverse recovery and it changes the *dI/dt* slope of the current. Moreover, as illustrated in Fig. 7(b) the voltage waveform is shifted in time and the peak of the voltage decreases. The *dV/dt* slightly decreases and this is one of the ways to prevent the avalanche breakdown in the device. This partially explains where the experimental measurements in Fig. 5 and Fig. 6 could not withstand higher switching rates at the rated current.

The physics of the failure mode during the reverse recovery of the body diode is investigated using the Fourier series reconstruction of the ambipolar diffusion equation. For better understanding the dynamics of failure, cross section view of a typical vertical MOSFET is illustrated in Fig. 8. In this diagram, the body diode and the parasitic BJT are separated using dashed lines. The p-well resistance (body resistance) is shown as *R* and the drain-base capacitance is shown as C_B.



(a)



(b)

Fig. 6 Experimental SiC MOSFET body diode reverse recovery waveforms at 13.4A/100V– Different gate resistances (a). Experimental SiC MOSFET body diode voltage waveforms at 13.4A/100V– Different gate resistances (b).

Fig. 9(a) to 9(e) shows the results of the simulations for 2 different *dI/dt*. As mentioned, the carrier lifetime of SiC is very small. Consequently, after switching the device off, the carrier stored in the drift region is rapidly extracted at a very high rate. Hence, the fast formation of the depletion region brings about a fast voltage rise with a very large *dV/dt* proportional to the switching rate and stray inductance (Fig. 9(b)). As mentioned previously the peak overshoot increases with increasing the switching rate. The electric field (Fig. 9(e)) at the junctions (PN^- and N^-N^+) cause the depletion width to start extending into the drift region. The result is that the drain-body capacitance decreases (Fig. 9(c)) and there is a resulting displacement current associated with the charging of

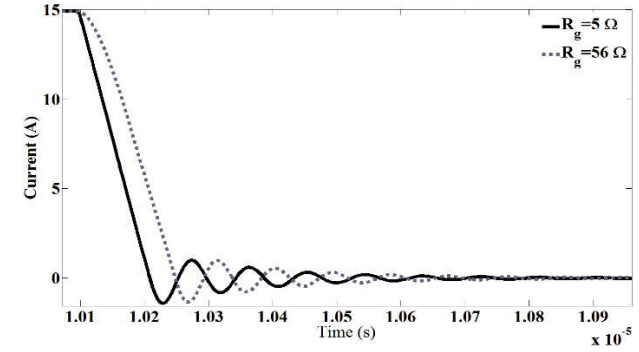
the capacitance (Fig. 9(d)). The depletion width and the drain-base capacitance can be calculated using (7) and (8) in which N_A and N_D are the donor and acceptor doping of the P and N$^-$ region respectively.

$$W_{d1} = -\frac{\varepsilon E_0}{q}\left(\frac{N_A+N_D}{N_A N_D}\right) \quad (7)$$

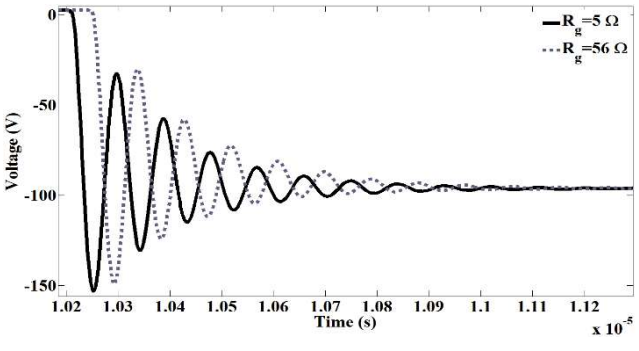
$$C_B = \frac{\varepsilon_i}{W_{d1}} \quad (8)$$

The displacement current at the PN$^-$ junction shown in Fig. 8 is the current which causes the parasitic BJT to latch-up if there is sufficient body resistance to forward bias the parasitic BJT. This brings about the avalanche breakdown of the device by causing a voltage drop across the emitter-base junction of the BJT greater than the in-built voltage (φ_{BE}). The displacement current is calculated below:

$$I_{disp} = \frac{\varepsilon A}{W}.\frac{dV_{DS}}{dt} = \left[\varepsilon A\sqrt{\frac{qN_{eff}}{2\varepsilon V_{CE}}}\right]\frac{dV_{DS}}{dt} \quad (9)$$



(a)



(b)

Fig. 7 Fourier series ADE simulation of the SiC MOSFET body diode turn-off current switched with different *dI/dt* (a). Fourier series ADE simulation of the SiC MOSFET body diode turn-off voltage switched with different *dI/dt* (b).

It can be seen from Fig. 9(d) that the average displacement current increases with the switching rate. This means that faster switching devices are more likely to undergo parasitic BJT latch-up. This is consistent with the experimental measurements in Fig. 6 and Fig. 7 where SiC body diodes were unable to withstand reverse recovery when switched with the lower gate resistance. The built-in voltage φ_{BE} of the parasitic BJT can be calculated:

$$\varphi_{BE} = \frac{KT}{q}\ln\left(\frac{P_+ n_-}{n_i^2}\right) \quad (10)$$

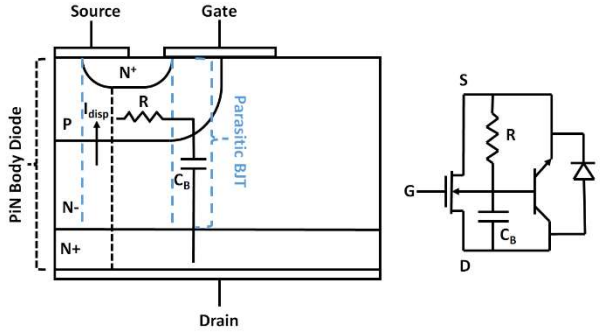


Fig. 8. Front view of a vertical MOSFET including the parasitic BJT and a body diode (Left) Equivalent circuit of a MOSFET with the parasitic BJT and a body diode (Right)

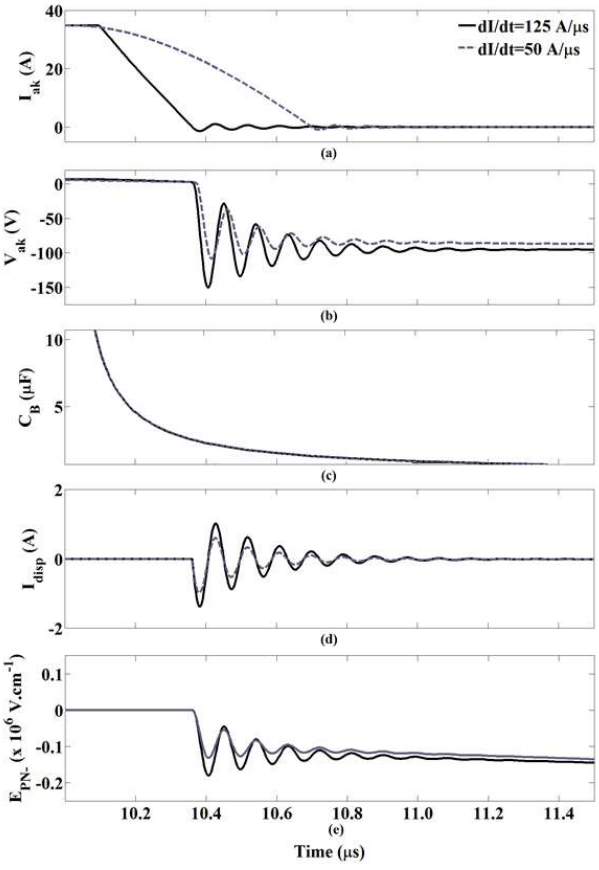


Fig. 9. F.S ADE result of the SiC MOSFET body diode displacement current, parasitic BJT base capacitance and electric field at P+N- junction during turn-off.

The critical MOSFET parameter that contributes to avalanche breakdown is the body resistance, which must be minimized for a rugged MOSFET. With adequate knowledge of the body resistance, the F.S ADE can be used as a diagnostic tool to investigate the limitations of the device.

V. CONCLUSION

The reliability of SiC MOSFET body diodes during reverse recovery was investigated. Experiments were carried out on Cree SiC MOSFET body diode and they showed the possibility of the device avalanche breakdown at high switching rates. Modelling of SiC MOSFET PiN body diode using F.S ADE indicates that the main parameters affecting the current and the voltage during the reverse recovery are switching rate or *dI/dt* of the device. At higher switching rate, the high *dV/dt* and the larger displacement current in the base of the parasitic BJT causes an avalanche breakdown of the MOSFET. This effect can be increased by increasing the working temperature. The model developed can be used by application engineers to investigate the reliability of SiC devices.

ACKNOWLEDGMENT

The author would like to thank Mr. Luke Evans and Dr. Alexandros Michaelides for their help. This work was sponsored by EPSRC in collaboration with Jaguar Land Rover PLC.

REFERENCES

[1] C. Xu, L. Xing-Ming, J. K. O. Sin, and K. Bao-wei, "Improving the CoolMS™ body-diode switching performance with integrated Schottky contacts," in *Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD '03. 2003 IEEE 15th International Symposium on*, 2003, pp. 304-307.

[2] T. Funaki, M. Matsushita, M. Sasagawa, T. Kimoto, and T. Hikihara, "A Study on SiC Devices in Synchronous Rectification of DC-DC Converter," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, 2007, pp. 339-344.

[3] D. De, A. Castellazzi, A. Solomon, A. Trentin, M. Minami, and T. Hikihara, "An all SiC MOSFET high performance PV converter cell," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-10.

[4] C. D. Brown and B. Sarlioglu, "Reducing switching losses in BLDC motor drives by reducing body diode conduction of MOSFETs," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 4286-4293.

[5] Z. Jun, C. F. Wheatley, R. Stokes, C. Kocon, and S. Benczkowski, "Optimization of the body-diode of power MOSFETs for high efficiency synchronous rectification," in *Power Semiconductor Devices and ICs, 2000. Proceedings. The 12th International Symposium on*, 2000, pp. 145-148.

[6] R. Siemieniec, O. Blank, M. Hutzler, L. J. Yip, and J. Sanchez, "Robustness of MOSFET devices under hard commutation ofthe body diode," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-10.

[7] Y. Shaoyong, A. Bryant, P. Mawby, X. Dawei, L. Ran, and P. Tavner, "An Industry-Based Survey of Reliability in Power Electronic Converters," *Industry Applications, IEEE Transactions on,* vol. 47, pp. 1441-1451, 2011.

[8] A. Bryant, "Simulation and Optimisation of Diode and IGBT Interaction in a Chopper Cell," Doctor of Philosophy, Queens' College, University of Cambridge, Cambridge, 2005.

[9] G. M. Buiatti, F. Cappelluti, and G. Ghione, "Power PiN diode model for PSPICE simulations," in *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE*, 2005, pp. 1911-1916 Vol. 3.

[10] L. Lu, S. G. Pytel, E. Santi, A. T. Bryant, J. L. Hudgins, and P. R. Palmer, "Physical modeling of forward conduction in IGBTs and diodes," in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, 2005, pp. 2635-2642 Vol. 4.

[11] A. T. Bryant, L. Liqing, E. Santi, P. R. Palmer, and J. L. Hudgins, "Physical Modeling of Fast p-i-n Diodes With Carrier Lifetime Zoning, Part I: Device Model," *Power Electronics, IEEE Transactions on,* vol. 23, pp. 189-197, 2008.

[12] L. Lu, A. Bryant, E. Santi, J. L. Hudgins, and P. R. Palmer, "Physical Modeling and Parameter Extraction Procedure for p-i-n Diodes with Lifetime Control," in *Industry Applications Conference, 2006. 41st IAS Annual Meeting. Conference Record of the 2006 IEEE*, 2006, pp. 1450-1456.

[13] A. T. Bryant, G. J. Roberts, A. Walker, and P. A. Mawby, "Fast Inverter Loss Simulation and Silicon Carbide Device Evaluation for Hybrid Electric Vehicle Drives," in *Power Conversion Conference - Nagoya, 2007. PCC '07*, 2007, pp. 1017-1024.

[14] A. T. Bryant, P. R. Palmer, E. Santi, and J. L. Hudgins, "Simulation and Optimization of Diode and Insulated Gate Bipolar Transistor Interaction in a Chopper Cell Using MATLAB and Simulink," *Industry Applications, IEEE Transactions on,* vol. 43, pp. 874-883, 2007.

[15] A. T. Bryant, K. Xiaosong, E. Santi, P. R. Palmer, and J. L. Hudgins, "Two-step parameter extraction procedure with formal optimization for physics-based circuit simulator IGBT and p-i-n diode models," *Power Electronics, IEEE Transactions on,* vol. 21, pp. 295-309, 2006.

[16] A. Bryant, N. A. Parker-Allotey, D. Hamilton, I. Swan, P. A. Mawby, T. Ueta*, et al.*, "A Fast Loss and Temperature Simulation Method for Power Converters, Part I: Electrothermal Modeling and Validation," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 248-257, 2012.

[17] P. A. Mawby, P. M. Igic, and M. S. Towers, "Physically based compact device models for circuit modelling applications," *Microelectronics Journal,* vol. 32, pp. 433-447, 5// 2001.

[18] P. M. Igic, P. A. Mawby, M. S. Towers, and S. Batcup, "Dynamic electro-thermal physically based compact models of the power devices for device and circuit simulations," in *Semiconductor Thermal Measurement and Management, 2001. Seventeenth Annual IEEE Symposium*, 2001, pp. 35-42.

[19] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*: Springer, 2010.

[20] A. T. Bryant, P. R. Palmer, E. Santi, and J. L. Hudgins, "A Compact Diode Model for the Simulation of Fast Power Diodes including the Effects of Avalanche and Carrier Lifetime Zoning," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, 2005, pp. 2042-2048.

[21] P. A. Mawby, A. T. Bryant, P. R. Palmer, E. Santi, and J. L. Hudgins, "High Speed Electro-Thermal Models for Inverter Simulations," in *Microelectronics, 2006 25th International Conference on*, 2006, pp. 166-173.