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A 1200V DC-link Hybrid Si/SiC Four-level ANPC Inverter with Balanced Loss Distribution, $dv/dt$ and Cost

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Abstract—To meet the aggressive performance targets of next-generation EV drivetrains, the traction inverter has been evolving by employing emerging technologies such as Silicon Carbide (SiC) devices and multilevel topologies. The four-level ANPC topology comprising six switches per phase has emerged as a promising solution for 1200V dc-link EV systems since its voltage balancing problem has been completely resolved by the latest control schemes. As the inherent property of this topology, the device power losses mainly concentrate on the two outer (primary) devices, which poses challenges to thermal management. This work proposes a hybrid Si/SiC configuration for this topology to achieve balanced overall performance. The SiC devices are adapted to combat the primary loss sources only, i.e. the two outer switches. Meanwhile, the other four switches staying as Si devices can offer additional benefits, on top of reduced cost, such as better loss/temperature distribution and reduced EMI and $dv/dt$ issues. These benefits of the hybrid configuration are demonstrated in a comparative study with simulation and FEA thermal analysis. A prototype has been built and tested to validate the concept.

Keywords—multilevel converter, Silicon Carbide, hybrid, four-level, propulsion inverter

I. INTRODUCTION

Propulsion inverters in Electric Vehicles (EVs) are expected to achieve aggressive performance indexes by 2035, such as $<1.75$ kW of cost, $>97$% of efficiency and $>25$ kW/kg of power density, as defined in the UK roadmap [1]. Meanwhile, EV systems also see a trend of increasing the voltage (e.g. from 400V to 800V/1200V) to reduce the weight of cables and enable faster charging. Towards these targets, propulsion inverters have been evolving by employing emerging technologies such as Silicon Carbide (SiC) devices and multilevel topologies. [2] reported a novel solution employing all-Silicon-Carbide (all-SiC) and four-level active neutral point clamped (4L-ANPC) topology [3], [4], which employs mature 1200/1700V SiC half-bridge modules to realize an efficient power conversion with a 1200V dc-link voltage. However, [2], [4] revealed that the power loss distribution among devices in this configuration is significantly uneven, which is the inherent property of the 4L-ANPC topology. This uneven loss distribution is undesirable in multilevel converters as established in [5]–[11], which poses challenges in the thermal design and limits the converter performance. Moreover, because over 60% of the power loss is concentrated on the primary (outer) modules in the all-SiC+4L-ANPC configuration as reported in [2], only 20% loss on each of the secondary (inner) modules appears to question the meaningfulness and necessity of employing the costly SiC devices for all of them. Additionally, the all-SiC solution also brings other disadvantages such as the high $dv/dt$ issues due to the fast switching of SiC devices which can lead to EMI issues, insulation stress and motor terminal overvoltage [12]. Therefore, this work intends to propose a hybrid Si/SiC configuration for the 4L-ANPC topology and investigates its performance gain.

As the contribution, this work demonstrates that, with a 4L-ANPC topology, a hybrid Si/SiC configuration is not just a cost-effective compromise to the all-SiC option. Compared to the all-SiC alternative, the hybrid solution offers additional benefits on top of the reduced cost, such as better loss distribution and reduced $dv/dt$ and EMI issues, while it slightly trades off the efficiency. The hybrid Si/SiC+4L-ANPC configuration can offer a balanced performance-cost gain over the all-Si and all-SiC options, which makes it an attractive solution to the 1200V dc-link traction inverter. Although the 4L-ANPC topology and the concept of a hybrid Si/SiC setup are not novel on their own, this work uniquely demonstrates the benefits of the hybrid solution that takes advantage of the special properties of the 4L-ANPC topology, which is supported and justified through a comparative study against the all-SiC and all-Si alternatives. This work is also complementary to previous studies on hybrid Si/SiC three-level ANPC converters [13]–[15].

II. DESIGN AND OPERATION OF A 4L-ANPC INVERTER

A. 4L-ANPC topology

Fig. 1 shows the 4L-ANPC topology formed by hybrid Si/SiC devices. Thanks to the topology’s “fractal” structure, it can be formed by three half-bridge power modules. Compared

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Fig. 1. Hybrid Si/SiC 4L-ANPC converter with three half-bridge modules.
to the three-level ANPC topology [3], this topology has the same
number of power devices, i.e. six devices per phase, while it
outputs one additional power level to further reduce the
switching voltage and filtering requirements. The operation of a
4L-ANPC converter is represented in Table I, which outputs
four voltage levels.

<table>
<thead>
<tr>
<th>Switch</th>
<th>Technology</th>
<th>Voltage rating</th>
<th>Current rating</th>
<th>Power module</th>
<th>$V_{FW}$ (V)</th>
<th>$R_{on}$ (mΩ)</th>
<th>$V_{FW}$ (V) @300 A</th>
<th>$E_{sw}$ (mJ) 600 V, 300 A</th>
<th>$R_{th,jc}$ °C/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1/S3</td>
<td>Si IGBT</td>
<td>1200 V</td>
<td>300 A</td>
<td>SKM00G012E4</td>
<td>IGBT</td>
<td>0.17</td>
<td>5.7</td>
<td>2.25</td>
<td>0.067</td>
</tr>
<tr>
<td>S2</td>
<td>SiC MOSFET</td>
<td>1700 V</td>
<td></td>
<td>CAS300M17BM2</td>
<td>Diode</td>
<td>0.9</td>
<td>4.0</td>
<td>2.11</td>
<td>0.17</td>
</tr>
</tbody>
</table>

B. Power Devices

As analyzed in [2], [16], considering a 1200 V dc-link
voltage, S1 and S3 in this topology both block and switch
at 400 V, while S2 blocks up to a static 800 V and switches still
at 400 V. In other words, the worst-case for S2 starts from blocking
a 400 V followed by a 400 V switching, which brings the voltage
across S2 to 800 V. Therefore, 1700V power modules are selected for S2 to leave a +112% margin (with reference to the
800 V static blocking voltage). Power modules for S1 and S3
are rated at 1200V to leave a +200% margin (with reference to
400 V switching voltage). The converter is designed against a
1200V dc-link for next-generation EV systems with a nominal
power rating of 100 kW and a sustained overload of 200 kW. The
selected power modules for the hybrid Si/SiC configuration are
dixed in Table II comparing the key parameters. It is
noticeable that the SiC MOSFET offers significantly lower
switching losses and better thermal conductivity for heat
dissipation. Both the SiC MOSFET modules and the Si IGBT
modules have identical footprint and housing (106x62x31 mm)
for the ease of assembly and experimental comparison.

C. DC-link Capacitor Voltage Balancing

The common dc-link of a multi-phase 4L-ANPC converter
comprises three capacitors C1, C2 and C3 in series. The 4L-
ANPC topology has an inherent voltage balancing issue that has
hindered its application in the past. As established in [17], [18],
if this topology is applied as a single-end inverter the middle
capacitor voltage will fully discharge under regular operation
without any auxiliary voltage balancer [19]. The auxiliary
balancer circuits are undesirable as they increase the complexity,
cost and power loss of the converter. Meanwhile, conventional
modulation-based voltage balancing approaches have
unneglectable limitations that prevent this topology to run at a
high modulation index and power factor.

Fortunately, advanced modulation schemes that emerged in
the past decade (e.g. [17], [20]–[23]) have completely solved
this topology’s limitation of operation region as an inverter. This
advance has enabled the 4L-ANPC topology to become a strong
candidate for low/medium voltage inverters (e.g. [16]). The
fundamental principle of these advanced modulation approaches is
to allow a third voltage level in one switching cycle, as shown in
Fig. 2(b), to gain extra control of the capacitor voltages. This
third voltage level is the “redundant level” that is redundant for
synthesising the reference voltage in a switching cycle, but it can
bring a new degree of freedom for voltage balancing. Hence this
approach is named redundant level modulation (RLM) [17].

D. Three-phase prototype design

To minimize the power loops and achieve a high power
density, the 3*3 power modules are placed to each other as close
as possible while leaving sufficient clearances. The layout of the
designed prototype is illustrated in Fig. 3. The dc-link is realized
with 3*3 film capacitors and laminated busbars to minimize the
parasitic inductance. The prototype sits on a forced-air-cooled
heatsink with a nominal thermal resistance of 0.07 K/W.

Fig. 2. Illustration of output voltage pattern in one carrier cycle with an equal
density, the 3*3 power modules are placed to each other as close
as possible while leaving sufficient clearances. The layout of the
designed prototype is illustrated in Fig. 3. The dc-link is realized
with 3*3 film capacitors and laminated busbars to minimize the
parasitic inductance. The prototype sits on a forced-air-cooled
heatsink with a nominal thermal resistance of 0.07 K/W.

Fig. 3. Layout design of the 1200V 100 kW Si/SiC 4L-ANPC prototype
III. COMPARATIVE CASE STUDY

This section presents a comparative study between the all-Si, proposed hybrid Si/SiC and all-SiC solutions to demonstrate the benefit of the hybrid configuration. As a reference, apart from the two devices selected in Table II, the 1700 V device in the all-Si case is assumed as SKM300GB17E4, and the 1200 V device in the all-SiC case is assumed as CAS300M12BM2.

A. Power Loss

The power loss and efficiency of the three cases are estimated in Simulink/PLECS based on the manufacturer datasheet assuming $T_J = 150^\circ C$. The results are visualized in Fig. 4. In the all-Si and all-SiC cases, it can be seen that the majority of the power loss concentrates in the two outer devices, i.e. the Module 2, which accounts for 65% of converter loss. This uneven distribution of power loss between power modules poses challenges to the thermal management. Additionally, this property also leads to an oversized heatsink for Module 1/3 because it is mainly sized against Module 2, which shows the highest temperature rise due to the concentrated loss.

This unevenness is further illustrated in Fig. 5. As can be seen, the all-SiC solution sees a 67%~72% loss difference between the outer module (Module 2) and the inner modules (Module 1/3). In contrast, the proposed hybrid Si/SiC solution can lower this difference to 16%~27% in the shown cases.

The estimated efficiency of the converter is plotted in Fig. 6 as a function of switching frequency, operating at 100 kW and 1.2 kV. It can be seen that the all-SiC option (blue trace) shows the highest efficiency as benefited from the low switching loss of SiC MOSFETs. Meanwhile, the hybrid Si/SiC option has slightly lower efficiency but it still sees a significant improvement to the all-Si solution. At 5 kHz, the hybrid Si/SiC solution only sacrifices 0.36% of efficiency compared to the all-SiC case (99.37% to 99.01%), while it greatly closes the loss difference gap as demonstrated in Fig. 5. At 25 kHz, the hybrid Si/SiC solution enjoys a 2% (2 kW) efficiency increase from the...
all-Si case (95.5% to 97.5%), while it is only 1% lower than the 98.5% of the all-SiC case. Note the results already included the effect of increased switching events caused by the redundant level modulation [17] to balance the capacitor voltages. In short, compared to the all-SiC solution, the proposed hybrid solution only mildly compromises the efficiency (~ 60% higher loss) while it achieves a better loss distribution.

**B. Thermal analysis**

Based on the predicted power loss in Fig. 4(a), a thermal analysis is conducted in ANSYS ICEPAK to estimate the steady-state temperature rise of the converter sitting on an air-cooled heatsink. In the simulation, the turbulent flow with a zero equation solver is applied. The thermal resistance from the junction to case and the thermal resistance of the thermal pad beneath each power module is represented by an equivalent thermal resistance. In addition, the power loss in each module is assumed to be evenly distributed between each paralleled chip, and is treated as constant over temperature. The results are shown in Fig. 7.

Fig. 7. Thermal performance simulated in ANSYS ICEPAK with the fan operating at $Q = 0.216 \text{ m}^3/\text{s}$, $P = 51.077 \text{ Pa}$

Fig. 7.1b shows that the all-SiC case leads to an uneven temperature rise between the module 2 part (left-hand side) and the module 1/3 part (right-hand side) on the heatsink surface, which is a nearly 10 °C difference. This temperature difference leads to the thermal stress on the heatsink between power modules. More importantly, assuming all six power devices in one phase are packed into one single power module, this uneven loss distribution would cause mechanical stress on the interconnections (e.g. bonding wires) and pose difficulties on the thermal management of the power module. In comparison, although the highest temperature rise is increased to 71.55°C due to the increased power loss of the Si IGBT that lifts the average temperature of the heatsink top, the hybrid Si/SiC configuration shows a much more even temperature distribution across the whole heatsink surface. There is nearly no temperature difference between the module 1/3 side and the module 2 side. Note although the hybrid setup leads to a more even loss distribution, the higher loss and lower thermal conductivity of Si IGBT devices can still prevent the converter from operating at a higher frequency without overheating (e.g. > 30 kHz depending on the cooling arrangement).
C. \(dv/dt\), EMI, overvoltage and insulation stress issues

The second benefit of the proposed hybrid configuration is the improved EMI performance and moderated \(dv/dt\) issues compared to the all-SiC option. The fast turn-on and turn-off time of SiC devices (e.g. 20 ~ 50 ns) leads to a high \(dv/dv\) on the converter output voltage (typically 15 ~ 30 kV/μs) that can cause severe EMI [24], insulation stress and motor terminal overvoltage due to the reflected wave phenomenon in the long-cable-fed motor drive system [12], [25]. A hybrid configuration is one approach to moderate this issue since the slower switching speed of the last-generation silicon-based switches acts as filters against the sharp edges. As shown in Table III, the switching actions associated with the output level change 4↔3 and 2↔1 occur on the IGBT modules in the proposed hybrid configuration, instead of the fast-switching SiC devices in the all-SiC case. In the cases switched by the Si devices, the converter output voltage steps see slower rising/falling edges (e.g. ~200 ns for turn-on and ~500 ns for turn-off) rather than the sharp edges generated by SiC devices. It should be highlighted that the voltage steps 4↔3 and 2↔1 are more crucial in Table III regarding the overvoltage and insulation issues, since they are associated with the peak of the output voltage (e.g. 4↔3 step is between \(+V_{dc}\) and \(+V_{dc}/3\), which are switched by Si IGBTs in the hybrid solution. Thus, qualitatively, the hybrid configuration can moderate the EMI and \(dv/dt\) issues by slowing down part of the output voltage steps.

| TABLE III SWITCHING DEVICES CORRESPONDING TO VOLTAGE LEVEL STEPS |
|-------------------|-----------------|-----------------|-----------------|
| Output voltage level change | 4↔3 \((\approx 25\%)\) | 3↔2 \((\approx 50\%)\) | 2↔1 \((\approx 25\%)\) |
| Hybrid Si/SiC | Si | SiC | Si |
| All-SiC | SiC | SiC | SiC |

*The share from total switching transitions with redundant level modulation

To further investigate this aspect, how frequent each of the voltage level steps occurs should be analyzed over fundamental cycles. As illustrated in Fig. 2(b), the redundant level modulation results in four voltage level steps and four switching transitions in each carrier cycle. As a simplification, the RLM is assumed to be constantly activated to balance the capacitor voltages as in [17]. In this case, over one fundamental cycle, the number of output voltage level steps can be calculated as

\[ n = f_{sw} / f_0 \cdot 4 \]

Given that there are always three voltage levels in one RLM-modulated switching cycle, two out of four voltage level steps are between level 3 and level 2, as illustrated in Fig. 8. The rest two transitions are either 4↔3 or 2↔1. Therefore, it can be deduced that over full fundamental cycles, 50% of voltage-level-change instances are 3↔2, which are associated with the switching of the outer switches S2/S2'. Due to asymmetry, the 4↔3 case and the 2↔1 case each occupies 25%, respectively. For example, with \(f_{sw} = 5 \text{ kHz}\) and \(f_0 = 50 \text{ Hz}\), there would be 200 instances of 3↔2 voltage step switched by the module 2 (SiC MOSFET), 100 instances of 4↔3 step switched by module 1 (Si IGBT) and 100 instances of 2↔1 steps switched by module 3 (Si IGBT) in one fundamental cycle. In other words, half of the total switching transitions and all of the peak-voltage-related switching transitions are slowed down by the Si IGBT devices in the hybrid setup. This analysis is verified in simulation and gives a qualitative justification of applying the hybrid Si/SiC setup to moderate the high \(dv/dt\) issues introduced by the SiC devices. Further evaluation will be conducted experimentally as future work to support this point.

![Fig. 8. Illustration of output voltage steps in the proposed hybrid Si/SiC + 4L-ANPC converter with redundant level modulation](image)

D. Cost of power devices

The third benefit of the hybrid Si/SiC option is the reduced cost, since only the primary devices (i.e. S2/S2') are upgraded to SiC devices. As presented in Table IV, the market price of SiC modules leads to an increase of the cost by a factor of five compared to the last-generation all-Si solution (from 8 $/kW to 39 $/kW). In comparison, the hybrid solution will moderate the cost to 21.8 $/kW, while it enjoys a significantly higher efficiency than the all-Si option (e.g. 2% higher at 25 kHz). Note this cost is only for the power devices. Compared to classic two-level converters, the increased device cost in the multilevel converter can be justified at a system level considering the lower cost from the decreased filtering/cooling components and the reduced cabling due to a higher voltage handling capability.

| TABLE IV REPRESENTATIVE POWER DEVICE COST IN OCTOBER 2021 |
|------------------|------------------|------------------|
| Configuration | Cost ($) |$/\text{kW} (\text{200kW}) |
| All-Si | 530 \(*3\) | 8.0 |
| Hybrid Si/SiC | 1,450 \(*3\) | 21.8 |
| All-SiC | 2,600 \(*3\) | 39 |

IV. EXPERIMENTAL VALIDATION

To validate the proposed hybrid Si/SiC 4L-ANPC converter configuration, a three-phase prototype has been built with the selected power devices listed in Table II. The gate drivers developed from commercial cores 2SC0650P with customized adapter boards, which are compatible with both the SiC MOSFET modules and the Si IGBT modules. The prototype is tested in a downscaled rig to prove the concept, of which the specifications are listed below.

| TABLE V DOWNSCALED TEST RIG SPECIFICATIONS |
|------------------|------------------|------------------|
| DC-link voltage and supply | 150 V, EA-PS 8600 |
| Carrier frequency \(f_{sw}\) | 5 kHz |
| Fundamental frequency \(f_0\) | 50 Hz |
| Modulation index \(M\) | 0.92 |
| Current sensor | LEM LA55-P |
| Voltage sensor | LEM LV25-P |
| \(R\) | 100 Ω per phase |
| \(L\) | 6.3 mH per phase |
A picture of the hybrid prototype is shown in Fig. 9, which shows the two types of power modules implemented, Si and SiC, their gate drivers, dc-link stacked busbars with capacitors, and the sensors for the closed-loop voltage balancing control.

The downscaled testing results prove the basic functionality of the proposed hybrid Si/SiC 4L-ANPC inverter. The prototype will be tested up to the full power level (1200 Vdc, 100 kW) to experimentally evaluate the thermal, \(dv/dt\), EMI and motor terminal overvoltage performance as future work.

V. CONCLUSION

This paper has proposed a hybrid Si/SiC 4L-ANPC inverter for 1200 Vdc EV propulsion applications and presented a reference design. Compared to the all-SiC counterpart, the proposed hybrid option is not just a cost-effective compromise, because it offers a better-balanced overall performance with more even loss distribution and moderated EMI and \(dv/dt\) issues by slightly trading off the efficiency. Taking advantage of the characteristics of the 4L-ANPC topology, costly SiC devices are employed to counter the primary loss sources only, i.e. the outer switches, while the rest of the devices are designed to stay as Si devices to avoid the high \(dv/dt\) related issues. This hybrid Si/SiC configuration has been justified in a comparative study against the all-SiC and all-Si alternatives. Further experimental testing will be conducted as future work to evaluate the benefits of the proposed configuration.

REFERENCES


