A Comparison of the Short Circuit Performance of 650 V SiC Planar MOSFETs, Trench MOSFETs and Cascode JFETs

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Abstract

Short circuits that occur in power converters put the power semiconductor devices under considerable electrothermal stress. The electrothermal stress causes a rise in junction temperature and ultimately device failure if the thermal limits of the device are exceeded. The device ruggedness under short circuit conditions is quantified by the short circuit withstand time (SCWT), which is the maximum duration the power device can dissipate the short circuit energy without failure. SiC MOSFETs are known to have reduced short circuit capability compared to comparatively rated silicon MOSFETs and IGBTs due to higher thermal impedance and reduced gate oxide robustness. In this paper, 650V rated SiC planar MOSFETs, Trench MOSFETs and Cascode JFETs have been subjected to short circuits with initial junction temperatures of 25°C, 75°C and 150°C. The results show the peak SC energy density (in mJ/mm^2) has a negative temperature coefficient for the Planar and Trench MOSFETs and is temperature independent for the Cascode JFET. The SCWT reduces with initial junction temperature for the SiC Planar and Trench MOSFET while showing less temperature dependency in the SiC Cascode JFET. The SiC Trench MOSFET demonstrates the highest SCWT although all devices show reduced SCWT compared to similarly rated silicon MOSFETs and IGBTs.

1 Introduction

Short circuits can occur in a converter due to shorting at the load side (called load under fault) or due to gate signal misfiring causing 2 devices in the same phase turning-ON thereby short circuiting the DC link (called hard switching fault). During the short circuit, the full load current flows through the device while the entire DC link voltage falls across it. This causes a significant amount of instantaneous power dissipation and rise in junction temperature. The magnitude of the peak short circuit current will be determined by the device switching rate and the more importantly, by the series inductance in the path of the short circuit current and the short circuit resistance of the device. The short circuit resistance should not be confused with the nominal ON-state resistance since the latter is related to normal operation (with low V_{DS}) and the former is related to anomalous operation (with high V_{DS}). During the short circuit, the rise in the junction temperature causes increased device resistance thereby causing the current through the device to reduce. The total short circuit energy will be determined by the magnitude and temperature coefficient of the short circuit resistance of the device.

SiC MOSFETs are known to have reduced short circuit capability compared to silicon MOSFETs. Two failure modes have been identified in SiC MOSFETs under short circuits. The first is related to the gate oxide failure while the 2nd is related to thermal runaway due to high junction temperatures in the MOSFET JFET region [1]. The reduced short circuit performance in SiC MOSFETs compared to silicon MOSFETs has partly been attributed to the reduced gate oxide reliability in SiC MOSFETs which causes higher gate leakage current during the short circuit [2-6]. Measurements have shown that thermal runaway from increased gate leakage current is the failure mechanism when short circuit measurements are performed at high drain-source voltages. When the measurements are performed at low drain-source voltages, the short circuit failure mode is gate oxide rupture [5]. Short circuit measurements have been performed on SiC MOSFETs with integrated Schottky barrier diodes used for body diodes (referred to as JMOS devices) and compared to conventional SiC MOSFETs with traditional body diodes [7]. The results showed reduced SCWT in the JMOS device although with both devices demonstrated SCWT higher than 5 µs. Studies of SCWT performance in SiC MOSFETs have shown improved performance with increased gate turn-off negative voltage and thicker gate oxides [8]. By increasing the turn-off gate voltage from -5 V to -10 V, it was demonstrated that the SC robustness of SiC MOSFETs was improved. Short circuit measurements have been performed on high voltage SiC devices useable in applications like solid state circuit breakers and medium voltage drives. In [9], short circuit measurements were performed on 3.3kV/400A SiC MOSFET modules and showed reduced SCWT (3 µs) compared to silicon IGBT modules. Short circuit measurements have also been performed on 10 kV SiC MOSFETs with 6kV DC link voltages [10]. The results showed a SCWT of 1.5 µs.

SiC Cascode JFETs are interesting devices because the device input is a silicon MOSFET, hence does not suffer from any of the drawbacks related to reduced gate oxide reliability in SiC MOSFETs. However, the design of the JFET and the internal connections between the JFET gate and the MOSFET source may cause a different failure mechanism under short circuits. In this paper, the short circuit performance of comparatively rated SiC Trench MOSFETs, SiC Planar MOSFETs and SiC Cascode JFETs have been assessed at different initial junction temperatures. Section 2 of the paper describes the experimental methodology showing the short circuit rest set up. Section 3 presents the short circuit measurements. Section 4 discusses the results and section 5 concludes the paper.

2. Methodology

The measurement set up comprises of the DC voltage source, the device under test (DUT), a series connected IGBT used to control the short circuit current and other components used to aid device switching and measurement. Figure 1 shows a picture of the test set-up while Figure 2 shows the corresponding circuit schematic. The control IGBT is a 1.7kV/1.2 kA device that is used isolating the DUT from the power supply in the event of failure. The IGBT turns on before the DUT and turns off after the DUT. Since the output capacitance of the IGBT is much larger than that of the DUT (400 nF vs 45 pF), the entire DC link voltage falls across the DUT.

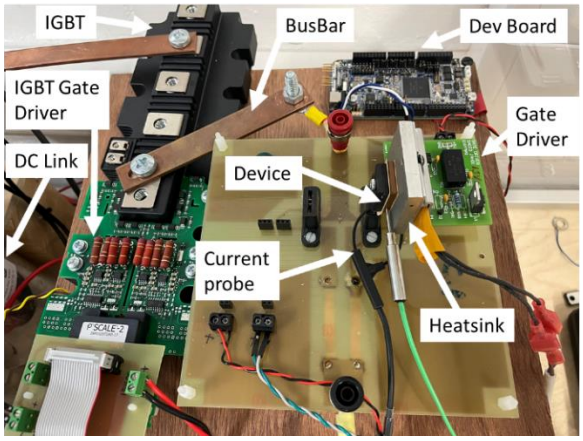

Figure 1. Picture of the Short circuit test circuit

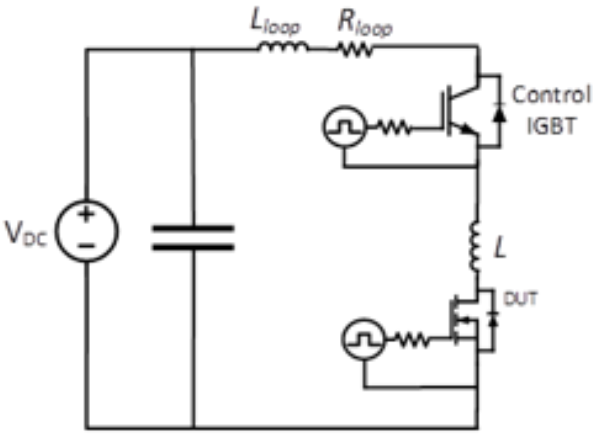

Figure 2. Circuit Schematic of the Short circuit test

Table 1 shows the devices under test (DUTs), the corresponding chip sizes in (mm^2) and their corresponding datasheet references.

Device	Size (mm^2)	I_{DS}(A)	Failure mode
SiC Planar (C3M0120065)	2.89	22	Gate-source (short) Drain-source (Fine)
SiC Trench (SCT3080AL)	6.25	30	Gate-source (short) Drain-Source (Fine)
SiC Cascode (UJ3C065080)	2.92	31	Gate-source (short) Drain-source (short)

TABLE 1. Devices under test for short circuit evaluation

Measurements are performed incrementally until device failure occurs. This is done by increasing the short circuit duration by 0.5 µs after each successful measurement. The short circuit measurements were performed on 3 devices from each technology to ensure statistical integrity of the measurements results.

3. Measurements and Results

Figures 3, 4 and 5 show the measured drain current, gate voltage and drain voltage from the SiC Cascode JFET. The SiC Cascode JFET fails in short circuit as indicated in Figure 3 where the current rises uncontrollably during the measurement. Subsequent failure analysis showed that all 3 terminals of the device were short circuited. In Figure 4, the gate voltage characteristics of the Cascode JFET remain steady at the turn-on voltage indicating that increased gate leakage during the test is not a problem. In the drain voltage characteristics shown in Figure 5, the undershoot during turn-on is due to parasitic inductance voltage negating the DC link voltage. As the device is turned off, due to the negative *dI/dt*, the polarity of the inductive overvoltage reverses itself and adds to the DC link, hence, there is a voltage overshoot as shown in Figure 5. As the device fails in short, it can be seen that the drain voltage drops at the instant that the current rises.

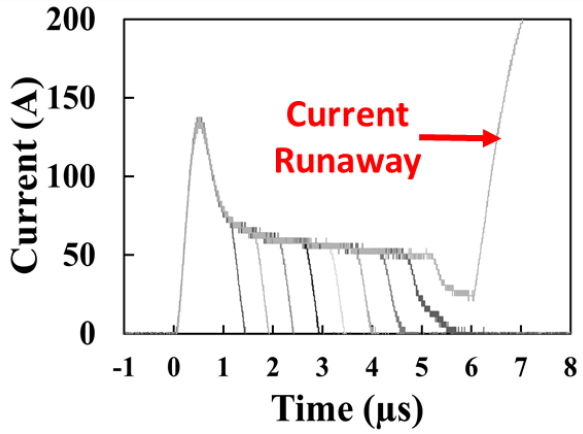

Figure 3. Short circuit current measured from 650V Cascode JFET

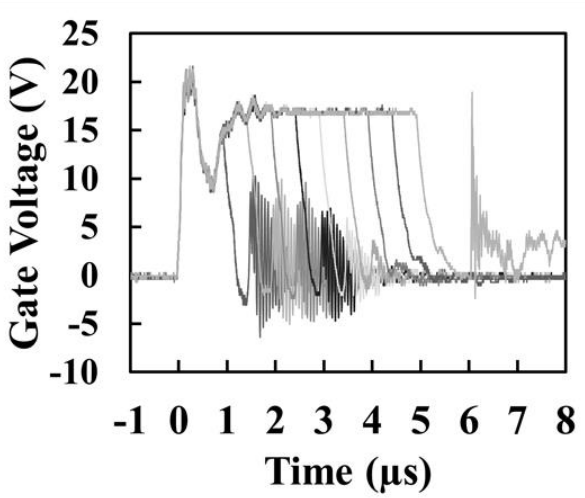

Figure 4. Gate voltage waveforms from SiC Cascode JFET during short circuit measurements

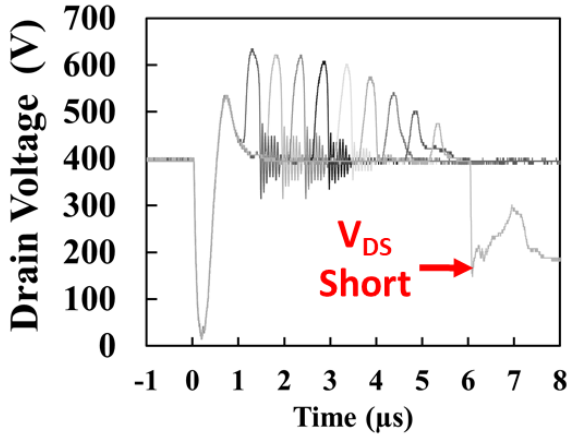

Figure 5. Drain-source voltage measurements from SiC Cascode JFETs during Short circuit measurements

Similar measurements are shown in Figure. 6 for the SiC planar MOSFET with an initial junction temperature of 25°C. Figure 7 shows the gate-source voltage measurements for the SiC planar MOSFET during the short circuit. It can be seen from Figure 7 that there is a reduction in the gate voltage as the short circuit duration is increased. This is due to the increased leakage current across the gate of the device. This leakage current results from thermally generated carriers at the drain end of the device gaining sufficient energy to scale across the oxide band-offset. As can be seen in Figure. 6, the SiC MOSFETs do not fail with current runaway but rather from gate-source terminal failure. This is unlike the SiC Cascode JFET where the failure is indicated by drain-source short circuiting followed by current runaway. Figure 8 shows the drain source voltage measured across the SiC planar MOSFET during the short circuit transient including the failure. There is no drain-source short circuiting as was the case for the SiC Cascode JFET as shown in Figure 5. Subsequent failure analysis on the SiC Planar MOSFET showed that the device was still capable of blocking a drain-source voltage even though the gate-source terminals were shorted circuited. The SiC Trench MOSFET also demonstrated an identical failure pattern to the SiC Planar MOSFET. However, the SiC Trench MOSFET demonstrated a short circuit withstand time almost twice that of the SiC Planar MOSFET. This is shown in Figure 9, where a short circuit withstand time of 11 µs is measured.

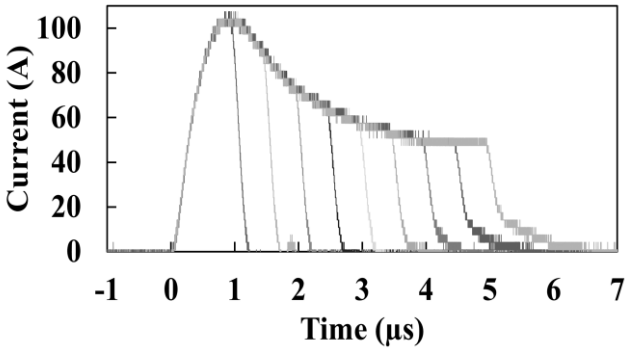

Figure 6. Short circuit current measurements for the SiC Planar MOSFET

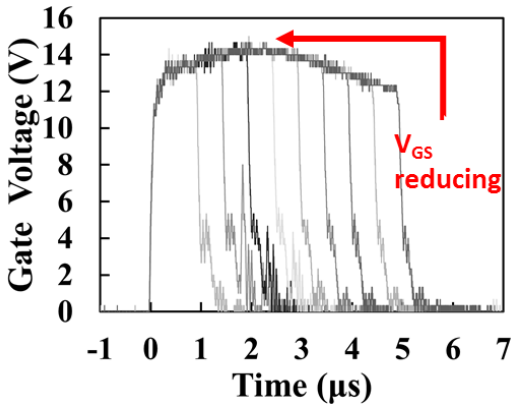

Figure 7. Short circuit gate-source voltage measurements for the SiC Planar MOSFET

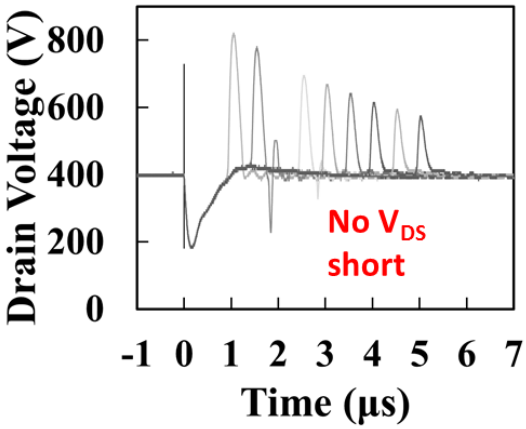

Figure 8. Short circuit drain-source voltage measurements for the SiC Planar MOSFET

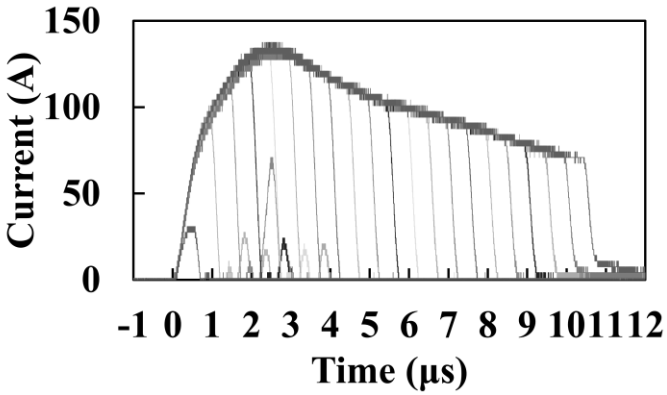

Figure 9. Short circuit current measurements for the SiC Trench MOSFET

4 Analysis

The last pass for all technologies is shown in Figure 10 together with a comparatively rated silicon IGBT with datasheet reference RGTH40TS65DGC11. It can be seen that the SiC Trench MOSFET exhibits the longest SCWT of the SiC devices. Due to the different chip sizes, further analysis is done by plotting the short circuit energy, peak short circuit current and the SCWT as functions of the chip size. Figure 11 shows that the peak short circuit current increases with chip size while Figure 12 shows the short circuit current density reduces with die size.

The short circuit critical energy density is defined as the maximum energy the DUT can dissipate without failure. This is calculated by simply integrating the short circuit power over the time duration for the last pass measurements. Figure 13 shows the short circuit critical energy density measured at different temperatures. Figures 11, 12 and 13 also show peak currents, current densities and energies at three different initial junction temperatures namely 25°C, 75°C and 150°C. It can be seen in Figure 11 that the peak short circuit current has a negative temperature coefficient in the Silicon IGBT while it is less temperature sensitive in the SiC devices. As the junction temperature is increased, the higher short circuit resistance reduces the peak short circuit current. However, due to the fact that SiC devices are less temperature sensitive than silicon devices (due to the wider bandgap in SiC), the short circuit characteristics are more temperature invariant in SiC devices.

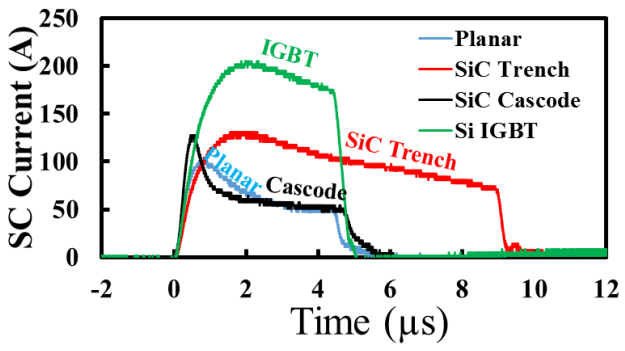

Figure 10. Last pass short circuit current measurements all technologies

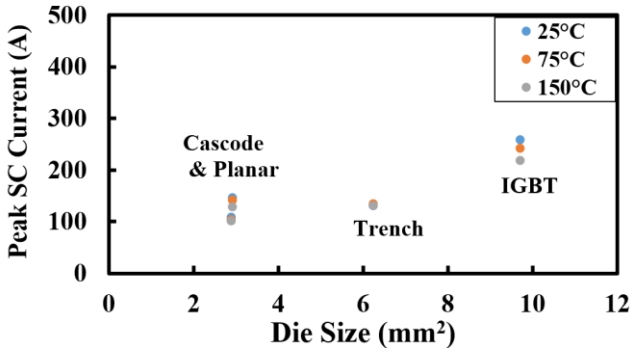

Figure 11. Peak Short circuit current as a function of die size for all technologies

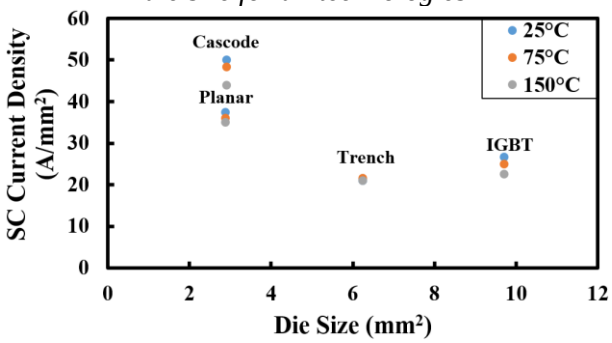

Figure 12. Peak Short circuit density current as a function of die size for all technologies

The short circuit energy density and short circuit withstand time show some temperature dependency in the SiC devices although less compared to the silicon IGBT. Figure 13 shows that the short circuit energy density reduces with temperature for all devices. However, in the case of the SiC Cascode JFET, there is less temperature dependency. Figure 14 shows the SCWT as a function of the die size for the different technologies where the SiC Trench MOSFET is the best performing SiC technology.

Comparing the switching energies of the SiC devices, the SiC Cascode JFET is the best performing device, followed by the SiC Planar MOSFET and the SiC Trench MOSFET. Since the parasitic capacitances determine switching speed and the these capacitances are directly proportional to die size, then it follows that there is a trade-off between short circuit withstand time and switching energy.

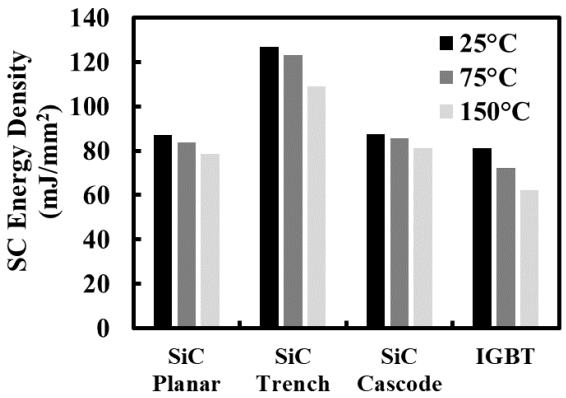

Figure 13. Short circuit energy density at different temperatures

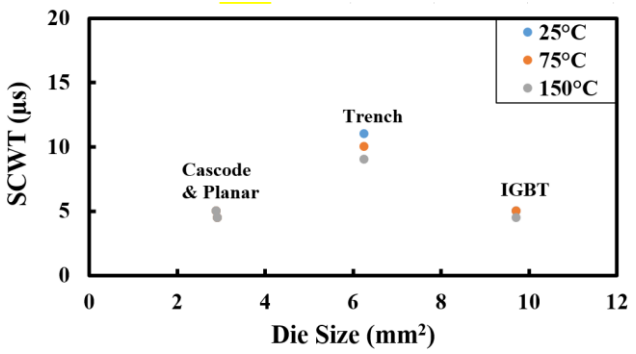

Figure 14. Short circuit withstand time as a function of die size for all technologies

5 Conclusions

Short circuit withstand time is an important metric for evaluating the robustness of power device technologies under short circuits. Comparisons of 650V SiC Trench MOSFETs, planar MOSFETs and SiC Cascode JFETs have been performed at different initial junction temperatures. The results show that the SiC Trench MOSFET has the highest SCWT although the SiC Cascode JFETs exhibit the highest short circuit energy density (in mJ/mm^2) followed by the SiC Planar MOSFET. There is a direct correlation between the switching energy and the SCWT with the device with the lowest switching energy (SiC Cascode JFET) exhibiting the smallest SCWT. Likewise, the device with the highest switching energy (SiC Trench MOSFET) exhibits the longest SCWT. The SiC Planar and Trench MOSFETs fail in the gate-source terminal without experiencing thermal runaway. In the case of the Cascode JFET, the device fails in thermal runaway likewise the silicon IGBT.

6 References

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