Progressive failure site generation in AlGaN/GaN high electron mobility transistors under OFF-state stress: Weibull statistics and temperature dependence

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Gate leakage degradation of AlGaN/GaN high electron mobility transistors under OFF-state stress is investigated using a combination of electrical, optical and surface morphology characterizations. The generation of leakage "hot spots" at the edge of the gate is found to be strongly temperature accelerated. The time for the formation of each failure site follows a Weibull distribution with a shape parameter in the range of $0.7 - 0.9$ from room temperature up to 120 ˚C. The average leakage per failure site is only weakly temperature dependent. The stress-induced structural degradation at the leakage sites exhibits a temperature dependence in the surface morphology, which is consistent with a surface defect generation process involving temperature-associated changes in the breakdown sites.

GaN-based high electron mobility transistors (HEMTs) have demonstrated extraordinary performance in RF and power electronics applications. However, the reliability of AlGaN/GaN HEMTs remains a challenge in their competition with technologies based on current materials such as Si or GaAs. OFF-state stress is known to result in an unrecoverable increase in gate leakage and a permanent decrease in output current.[1-7] The increased gate leakage current is believed to result predominantly from the formation of trap-assisted percolation paths in the AlGaN barrier,[2-5] which have also been linked to the appearance of multiple electroluminescence (EL) "hot spots" and surface structural defects on the drain side of the gate, indicating the location of the leakage paths.[8] Structural degradation on the device surface was initially ascribed to mechanical stress due to the inverse piezoelectric effect when the electric field exceeds a critical value.[9-11] However, similar gate degradation also occurs at lower bias with sufficiently long stress time[1,2,6,12] so a strict critical voltage for breakdown may not exist, contrary to expectations of the inverse piezoelectric effect. This has favored alternative mechanisms that may contribute to OFF-state gate degradation, such as current or electric field-driven electrochemical processes on the device surface.[13,14] It was recently shown that the increase of gate leakage and generation of gate-edge failure sites eventually saturate due to an exclusion zone formed around each failure site in which further defect formation is hindered.[15]

Temperature is known to affect reverse-bias leakage in Schottky contacts to AlGaN/GaN[16-18] and is thus expected to play a critical role in OFF-state HEMT degradation. Previous work reported a weak temperature dependence of time-to-breakdown (t_{BD}) for the gate.[2,6,7] These studies, however, focused only on device early failures, i.e. the appearance of the very first leakage path, which could be affected by processing-induced defects. Investigations of the temperature effect on the continuous generation of leakage paths beyond device early failures and associated structural degradation are still lacking. In this letter, we study OFF-state gate degradation by stressing devices beyond the occurrence of the first failure site. We identify the different stages in failure site generation using Weibull statistics. By means of gate leakage, EL emission and surface morphology analyses, the impact of temperature on the leakage path formation as well as the surface structural defect generation is studied. Based on the findings, a degradation model is proposed involving temperature-dependent leakage path formation and surface defect generation.

AlGaN/GaN HEMTs grown by metal-organic chemical vapor deposition (MOCVD) on SiC substrates were studied. The heterostructure consisted of a 1.9 μm GaN buffer layer and a 25 nm AlGaN barrier layer (25% Al content). Standard TiAlTiAu Ohmic and NiAu Schottky contacts were used for the source and drain electrodes and the gate electrode, respectively. The devices were passivated by a $SiN_x/SiO_2/SiN_x$ multilayer, and had a 4 μm source-drain gap, a 0.6 μm-long gate and a 1 μm source-to-gate distance. No field plate was used so the EL hot spots generated during stress could be spatially resolved from the device top surface. The devices were stressed for 7.5 hours at $V_{gs} = -15$ V (pinch-off voltage $V_{po} = -5$ V) and $V_{ds} = 40$ V at four different temperatures from room temperature up to 120 ˚C. During the stress the gate leakage current (I_g) was monitored and EL images were recorded using a high-resolution CCD camera.

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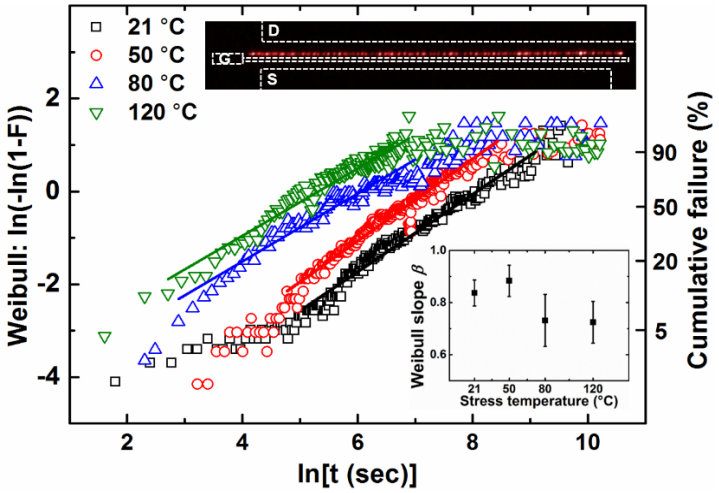

FIG. 1. Weibull plot of the generation time of each defect under stress V_{gs} = −15V, V_{ds} = 40V at different temperatures. The right vertical axis indicates the corresponding cumulative failure percentage. Insets: (Top) False color EL image of a stressed 100 μm-wide AlGaN/GaN-on-SiC HEMT. (Bottom) Weibull slope β extracted from the linear region of each curve.

The top inset of FIG. 1 shows a representative EL image of a 100 μm-wide AlGaN/GaN HEMT after 7.5 hours bias stress at T = 21 ˚C until the EL spot generation was saturated, i.e. the image shows the maximum attainable number of EL spots. These EL spots appeared on the drain-side edge of the gate where the electric field peaks, indicating the emergence of local percolative leakage pathways to the device channel. They were distributed along the entire gate finger in a nearly uniform pattern, and were sufficiently far apart to be individually distinguished. As widely used in silicon MOSFETs[19-22] and lately adopted in GaN-based materials,[2,6] the time-to-breakdown (t_{BD}) for gate degradation can be described by Weibull statistics in which the failure rate is proportional to a power of time. Instead of recording t_{BD} on a series of devices, we monitor the continuous emergence of EL spots at the gate edge on a single device and treat each EL spot as an independent failure site. The corresponding cumulative distribution function for Weibull statistics $F(t) = 1 - \exp[-(t/\eta)^{\beta}]$ can be readily calculated as the rank of each failure site in time. Here t is the time-to-failure for each EL spot, β is the shape parameter or Weibull slope that describes the change of failure rate over time, and η is the scale parameter that represents the characteristic failure time.

As illustrated in FIG. 1, heating the device during stress shifts the Weibull curves to shorter times, i.e. smaller η, meaning that the generation of defects is accelerated by temperature. Each of the Weibull curves appears to consist of three regimes with different slopes corresponding to different stages of degradation. At the beginning of stress, infant failures of a few spots occur and as they are weeded out over time, the failure rate decreases which is reflected in the smaller slope at short times. Early degradation is less distinguishable at higher temperatures when the initial generation of EL spots is too rapid to be resolved. The central region of each curve follows a Weibull distribution with a slope β ranging from 0.7 to 0.9 (FIG. 1 inset). In general, β is proportional to the trap generation rate and the critical density of traps in the gate dielectric needed to trigger the breakdown.[2,21] Taking into account the uncertainties in the linear fits, the extracted β has a weak temperature dependence, indicating that a common trap generation mechanism remains active from room temperature to 120 ˚C. This is consistent with distributions of t_{BD} for both silicon oxide[20-22] and AlGaN[2] on each of a series of devices in the same temperature range. Moreover, β obtained here is comparable to that (0.55 − 0.76) for AlGaN/GaN-on-Si HEMTs,[2] suggesting a similar failure mode in the two cases. Using the time for 63.2% failure on each of the devices, an activation energy of ~ 0.4 eV was extracted for the leakage path creation process. The fluctuation in data near the end of stress in FIG. 1 indicates the regime where failure site generation starts to saturate due to defect-defect interactions.[15]

It could be argued that the particular degradation pattern observed here such as the saturation of failure sites is caused by pre-existing defects or other material properties and would be strongly dependent on growth or processing. However, similar degradation behavior with a comparable density of failure sites after saturation was also observed on a GaN-on-GaN HEMT with substantially lower initial defect and dislocation densities.[23] The saturation of defect generation is therefore not caused by extrinsic defects but more likely by other self-limiting mechanisms.[15] This suggests a common failure mechanism for both GaN-on-SiC and GaN-on-GaN devices.

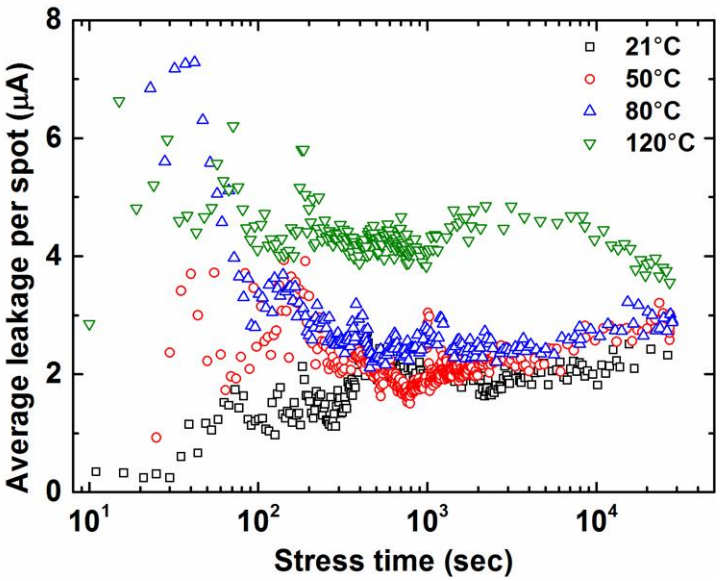

FIG. 2. Average leakage current per EL spot in the AlGaN/GaN HEMTs as a function of time at different stress temperatures. The errors are approximately ±10% (not shown) due to uncertainties in the counted number of EL spots.

It was previously shown that each of the generated spots contributes a similar amount of current to the total gate leakage while emitting a comparable EL intensity.[8] To better understand the effects of temperature on a generated percolation path, the gate leakage divided by the number of spots is therefore used to represent the average leakage current per failure site and plotted as a function of time in FIG. 2. The fluctuations at short stress times are primarily due to uncertainties in dividing a gradually changing current by an integer number that starts from zero. As more failure sites are generated, the average current converges to a reasonably steady value between 2 and 3 μA for devices stressed at 21 ˚C, 50 ˚C and 80 ˚C, and ~ 4 μA for the device stressed at 120 ˚C. The in-stress leakage current per spot averaged over time is presented in FIG. 3, showing only a marginal temperature dependence with a low activation energy of ~ 70 meV. This suggests that conduction through the leakage paths is weakly thermally activated. The post-stress gate leakage measured under the same bias at room temperature is reduced compared to that measured during stress at elevated temperatures due to lowered percolation conductance. Nevertheless, greater gate current is still noticeable for the 120 ˚C-stressed device at room temperature compared to devices stressed at lower temperatures, both under stress conditions and at lower voltages (FIG. 3 inset), which is possibly related to the preserved characteristics of the leakage paths.

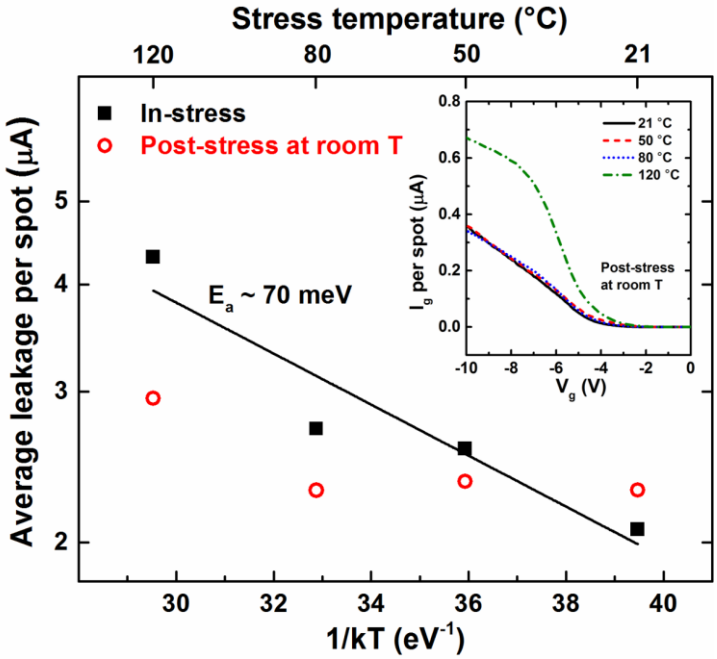

FIG. 3. Time-averaged in-stress leakage per spot and post-stress leakage per spot measured at room temperature. Inset: Post-stress Schottky gate characteristics (in linear scale) measured at room temperature.

After the stress, the passivation and metal contacts of stressed devices were removed by HF etching and aqua regia etching, respectively.[24] The source-drain gap over the entire gate width on each etched device was then scanned with an atomic force microscope (AFM). Representative images for devices stressed at 21 ˚C and 120 ˚C are shown in FIG. 4. Each of the generated defects left an imprint in the form of a surface pit on the drain side of the gate edge, corresponding to the location of a stress-induced leakage site.[8] The formation of similar pit defects at room temperature was attributed to current-driven surface electrochemical reactions studied in detail in Refs. 13 and 14. As illustrated in FIG. 4(a) and (b), a certain proportion of these pits have an elongated shape either perpendicular or parallel to the gate. The length and width of each pit were measured on the entire gate width of each stressed device. Based on the aspect ratio of each pit (the ratio of the dimension normal to the gate width compared to that parallel to the gate width), all pits are categorized into three types: One that appears normal to the gate finger (Type 1, aspect ratio > 2), one that does not have a distinctive orientation and is usually < 100 nm in either dimension (Type 2, 0.5 < aspect ratio < 2), and one along the finger (Type 3, aspect ratio < 0.5). As shown in FIG. 4(c), there tend to be more pits growing perpendicular to the gate finger at lower temperatures and more pits stretching along the gate finger at higher temperatures. Consequently, a temperature dependence of the average pit size is evident in the dimension normal and parallel to the gate width, respectively (FIG. 4(d)). The representative orientation of pits is consistent with previous observations under OFF-state stress at room temperature where the surface defects were shown to grow towards the drain over time,[15] or those under ON-state stress at elevated temperatures due to self-heating.[25] The temperature dependence of defect morphology, however, was never noted. The transition is particularly pronounced from 80 ˚C to 120 ˚C and the differences below 80 ˚C are only marginal, which implies possibly a nonlinear temperature dependence of such structural degradation.

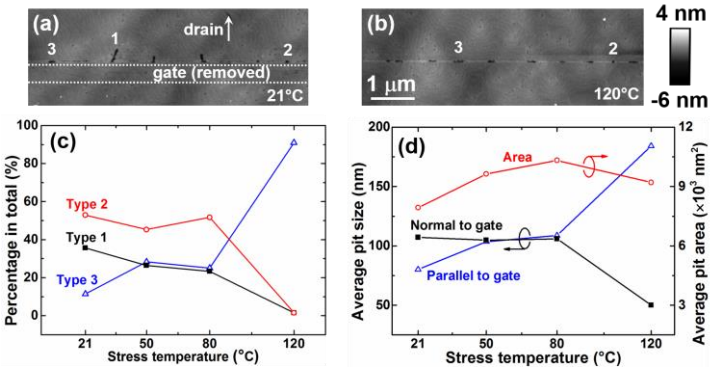

FIG. 4. Representative AFM images of AlGaN/GaN HEMT device surface after removal of the passivation and metal contacts for devices stressed at (a) 21 ˚C and (b) 120 ˚C, respectively. (c) Percentage of different types of surface pits, with Type 1 defined as those of aspect ratio > 2, Type 2 of aspect ratio between 0.5 and 2, and Type 3 of aspect ratio < 0.5. (d) Average pit area and average pit size in the dimension normal and parallel to the gate finger.

The observed characteristics of pit morphology are likely linked with the leakage path formation that triggers the surface defect generation. Prior to stress, there are no sizable pre-existing leakage paths although spatial inhomogeneities exist in the leakage current or field due to crystallographic irregularities or gate-edge roughness. This was indeed demonstrated by the non-uniform pre-stress EL intensity along the gate finger.[23,26] Upon OFF-state stress, traps are first generated at "weak" locations along the gate edge; when the density of traps is sufficiently large a percolative conduction path may be formed in the AlGaN layer via which electrons can flow to the device channel. It was shown in silicon oxide that percolation paths are formed at individual spots as traps are favorably generated in clusters due to a positive feedback process.[19,20] Likewise, in the case of AlGaN/GaN HEMTs, localized leakage sites are formed along the gate finger (FIG. 1 top inset). In the meantime, lowered barrier together with the leakage current activates the formation of structural defects, presumably due to an electrochemical process occurring on the surface.[13-15] At lower temperatures, some defects tend to grow towards the drain contact (FIG. 4(a)), presumably following the high potential gradient on the device surface. The tip of such a defect has a small radius of curvature and thus intensified field, allowing the defect to further grow. At higher temperatures (120 ˚C in particular), the initial spatial barrier height fluctuation would be smeared out by the increased thermal energy, resulting in less localized or spatially broader breakdown sites, and thus the wider pits in FIG. 4(b).

Additionally, heating may also contribute to the broader breakdown sites by enhancing the trap clustering in forming the percolation paths,[20] although there is no clear evidence that the leakage paths are wider throughout the entire AlGaN layer at elevated temperatures. In fact, structural degradation is limited to near the AlGaN surface with the pits being only a few nanometers deep (FIG. 4(a)(b)). Moreover, despite a certain amount of structural defects growing in two distinct directions during the stress, the average current through each site

remains reasonably constant over time as shown in FIG. 2. This suggests that the leakage paths are likely localized during stress as the surface defects grow in size over time, rather than flowing through the entire failure site area. For a Type 1 defect, the leakage path likely locates near the far end of the defect where the enhanced field screens the original gate edge, whereas for a Type 3 defect, field intensification and preferential current flow would occur at both ends of the defect on the gate edge. This is consistent with the post-stress leakage (FIG. 3) as well as the Schottky gate characteristics (FIG. 3 inset), where the 120 ˚C-stressed device having a higher percentage of Type 3 defects has a greater leakage through each failure site than the other devices (FIG. 4(c)); the contrast in I_g per spot between devices is in reasonable accordance with the percentages of the two types of elongated defects differently orientated.

While the surface pits have distinct morphologies, the average area of a surface pit on each of the stressed devices shows only a marginal temperature dependence (FIG. 4(d)). An Arrhenius relation therefore does not hold between the average pit volume and temperature, unlike what was observed for ON-state stress-induced structural degradation due to a diffusion process.[25] This may be evidence for a self-limiting mechanism responsible for the saturation of failure site generation as aforementioned. For example, assuming that an electrochemical process dominates the structural degradation, the failure site generation could be limited by the availability of electrochemically active species around each failure site.[14,15]

In conclusion, the impact of temperature on OFF-state gate degradation of AlGaN/GaN HEMTs has been studied. An electroluminescence-based approach for failure analysis is demonstrated, which monitors the progressive generation of failure sites at the edge of the gate in each stage of the degradation on a single device. This enables the understanding of physics beyond device early degradation. The failure site generation is a temperature-accelerated process that can be described by Weibull statistics with a slope $\beta = 0.7 - 0.9$ weakly influenced by temperature; this suggests that a common trap generation mechanism remains active in forming the percolation paths at different temperatures. The average leakage current per spot is only weakly thermally activated with an activation energy of ~ 70 meV. After the removal of passivation and contacts, the pit defects revealed by AFM exhibit a distinct temperature dependent morphology. The pits generated at lower temperatures are either small or have an elongated shape towards the drain contact, whereas the pits generated at 120 ˚C tend to extend along the gate edge. It is proposed that heating affects the spatial distribution of barrier height, resulting in temperature dependent structural breakdown triggered by the leakage path formation. The defect morphology together with the gate current flowing through each failure site offers insight into the location where leakage occurs.

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