# Influence of Supply Voltage on the Multi-Cell Upset Soft Error Sensitivity of Dual- and Triple-Well 28 nm CMOS SRAMs

Balaji Narasimham, Jung K. Wang, Narayana Vedula, Saket Gupta, Brandon Bartz, Carl Monzel
Broadcom Corporation
Irvine CA, USA
balajin@broadcom.com

Indranil Chatterjee
University of Bristol, Bristol, UK

Bharat L. Bhuva, Ronald D. Schrimpf, Robert A. Reed
Vanderbilt University
Nashville TN, USA

***Abstract*—Dual- and triple-well bulk CMOS SRAMs fabricated at the 28-nm node were tested using alpha particles and heavy-ions over a range of supply voltages. Dual-well SRAMs have better Multiple Cell Upset (MCU) cross sections and spread for nominal voltage, while triple-well SRAMs are better for reduced voltages. TCAD simulations show that single-event upset reversal due to charge confinement is responsible for improved soft error rate (SER) performance at low voltage operation for triple-well SRAMs.**

***Keywords: alpha particle, dual-well, heavy ion, linear energy transfer (LET), MCU, soft error rate( SER), SRAM, triple-well.***

## I. INTRODUCTION

With technology scaling and the integration of high-speed digital, analog, and RF components on monolithic ICs, reduced substrate noise coupling and cross-talk between subcircuits is required for reliable circuit operation. One of the approaches to address these concerns is to use triple-well technology. Another major concern for designers is the overall power requirements for a circuit. Since dynamic power is proportional to $V_{DD}^2$, system-level designers have resorted to reducing supply voltage to reduce power requirements [1]. However, using triple-well technology in conjunction with reduced supply voltages has the disadvantage of increasing the soft error rate (SER). Moreover, technology scaling and increased packing densities have resulted in soft errors becoming one of the key reliability concerns for advanced technology nodes [2]. In different studies on the impact of triple-well technology on the SER [3–5], some have shown that triple-well architecture yields higher Multiple Cell Upset (MCU) rates [4], while other studies have indicated reduced SRAM SER for triple-well designs for high-LET particles [5]. A recent study concluded that charge confinement along with well doping and layout spacing strongly influences overall SER performance for SRAMs [6]. Most of these studies are focused on single-bit SER, but single-bit SER does not yield a complete picture of SRAM SER vulnerability. MCUs are increasingly becoming the determinant of SRAM reliability due to the high density of transistors in an SRAM design. Although designers have adopted error-correcting code (ECC) and interleaving as standard techniques to mitigate soft errors, the efficacy of these techniques depends on the extent of MCU rates [7, 8]. Bit interleaving also adds complexity to the design, impacting area and power consumption, and may not be practical for some memory types [7]. And as discussed in [8], if the size of a multi-cell cluster is larger than the memory interleaving distance, detected unrecoverable errors (DUE), or silent data corruption (SDC) can occur. Thus, it is important to evaluate the MCU SER for SRAMs that operate at reduced voltages.

In this work, the MCU SER performance of triple-well and dual-well SRAMs fabricated in a 28-nm commercial bulk CMOS process was tested with alpha particles and heavy ions over a range of supply voltages. Experimental results indicate that, while triple-well architecture has a higher MCU cross

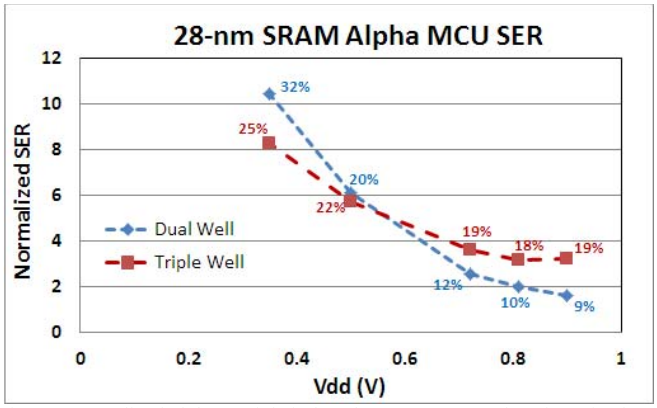


Fig. 1. Normalized alpha particle induced MCU SER as a function of voltage for dual- and triple-well devices. The data labels indicate the proportion of MCU event rate as a percentage of overall SE events.

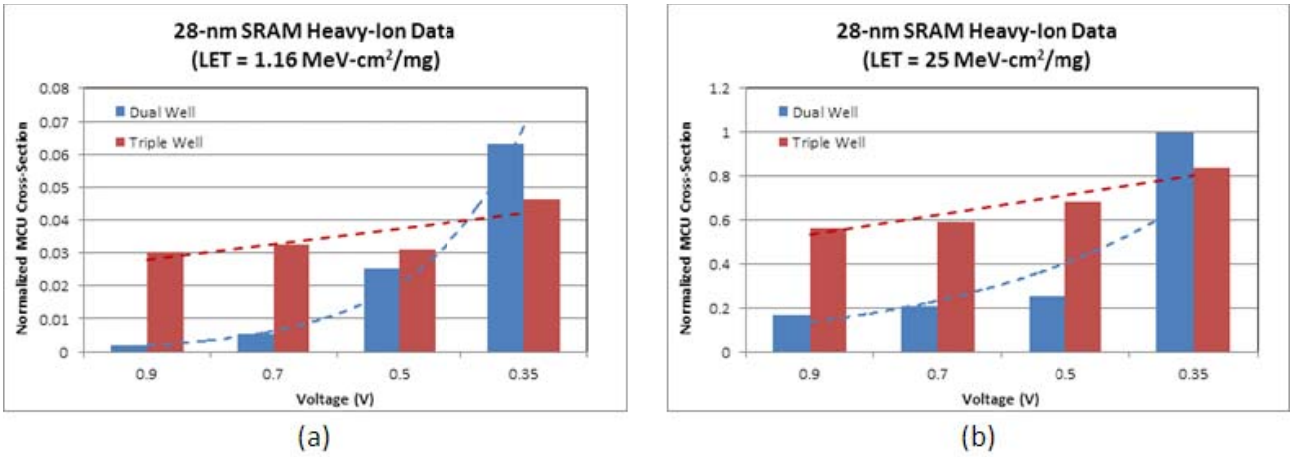


Fig. 2. Normalized heavy-ion cross section as a function of voltage for (a) an LET of 1.16 MeV-cm$^2$/mg and (b) an LET of 25 MeV-cm$^2$/mg.

section than dual-well for nominal voltage operation [6], the trend is reversed at reduced voltages. TCAD simulations indicate the dominance of the upset-reversal mechanism [5, 6, 9] for triple-well SRAMs at reduced voltages as the primary mechanism for this behavior. These results will help identify the range of supply voltages for which dual- or triple-well designs will offer superior SER performance.

## II. 28-NM ALPHA AND HEAVY ION TEST RESULTS

Dual- and triple-well SRAMs with similar design and layout were fabricated in a commercial 28-nm bulk CMOS process. The supply voltage needed for data retention was found to be as low as 0.3 V. This enabled conducting very low supply voltage tests whereby the data were written at nominal voltage and the supply voltage was then reduced for radiation tests, which is similar to a standby mode in practical applications. Following the radiation exposure, the supply voltage was brought to nominal level for data reading. Multiple runs without radiation were conducted to verify stable operation at each voltage level.

Alpha particle tests were conducted using an Am-241 foil with an activity of 0.1 µCi. Data were collected for different test patterns and over a range of supply voltages. Fig. 1 shows the normalized, alpha particle-induced MCU SER as a function of supply voltage. The data labels indicate the proportion of the MCU event rate as a percentage of the overall SE events. Because MCU rates are major determinants of SRAM SER reliability, they provide a better comparison of dual-well versus triple-well technologies than single-bit upsets. When supply voltage is reduced, the contribution of MCUs increases more rapidly for the dual-well SRAM compared to the triple-well SRAM. For the dual-well SRAM, the contribution of MCUs increases from 9% at nominal voltage to 33% at 0.35V of overall SER; for the triple-well SRAM, the MCU contribution increases from 19% at nominal voltage to 25% at 0.35 V. The difference in the rate of increase in the SER is primarily due to the dominance of the upset-reversal mechanism (also called reinforced charge collection) at reduced supply voltage operation for triple-well SRAM designs [5, 6, 9].

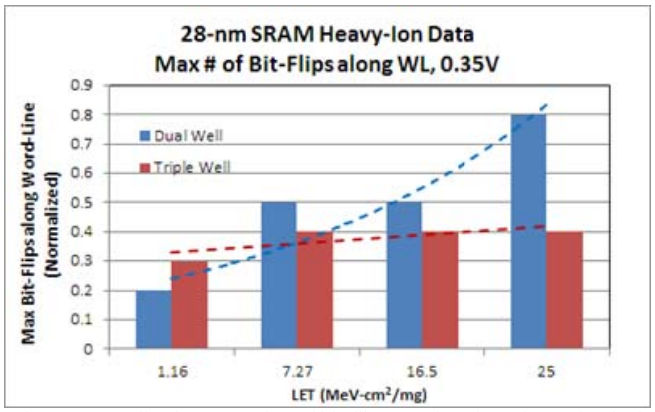


Fig. 3. Normalized max number of bit-flips as a function of LET for dual and triple-well devices.

Heavy ion tests were performed at Lawrence Berkeley National Laboratory with a 16 MeV/nucleon cocktail using particles with linear energy transfer (LET) ranging from ~1 to 25 MeV-cm$^2$/mg. Fig. 2(a) shows the normalized heavy ion MCU cross section of the dual- and triple-well SRAMs for a low-LET ion incident normally to the die. Fig. 2(b) shows the same for a relatively high-LET ion, also incident normally to the die. In both cases, the dual-well MCU cross section increases exponentially at low voltage (0.35 V), but the triple-well cross section increases only slightly. Moreover, at 0.35V the dual-well MCU cross-section trends higher than the triple-well cross-section for both LET cases.

The maximum number of bit-flips in a word-line (which determines the efficacy of ECC), shown in Fig. 3, was found to be significantly smaller for triple-well designs at reduced voltage operation compared to dual-well designs across a range of LETs. These results make clear that triple-well designs will have better soft-error reliability than dual-well designs for supply voltages lower than ~0.5 V. While the general trends are technology-independent, the technology node and nominal voltage is likely to influence specific results. In addition, the effect of charge confinement, and hence bit-reversal, has been proven to be higher for angular strikes [5]. Thus in real environments, where particles will impinge at different angles, triple-well designs are likely to be more effective at higher

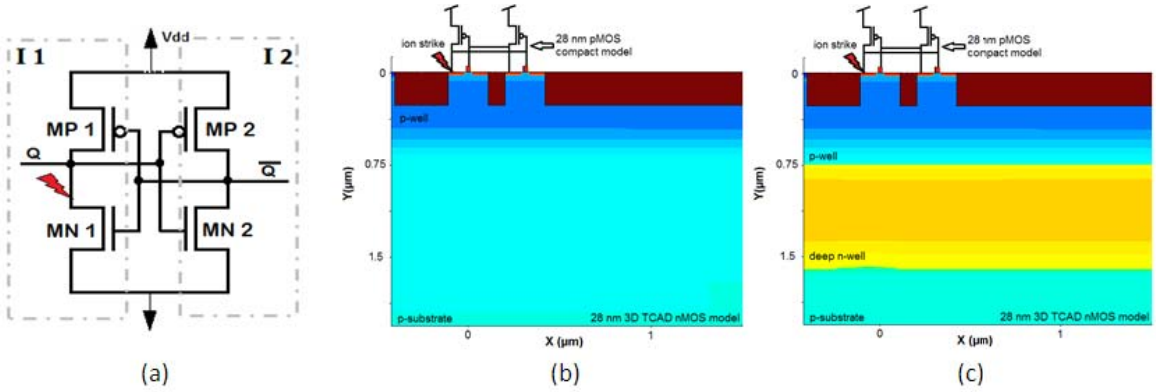


Fig. 4. (a) Schematic of the mixed-mode TCAD simulation setup, (b) 2D cut of dual-well and (c) 2D cut of triple-well NMOS TCAD model.

voltages than what was observed in the results here for heavy ions. This is also observed from a comparison of the alpha SER test results (where the particles also impinge at different angles), to the low-LET heavy-ion tests performed at normal incidence to the die. The dual-well alpha MCU SER crosses over the triple-well alpha MCU SER at 0.5 V, while in the case of the heavy-ion data the cross-over occurs at <0.5 V.

## III. 3D-TCAD Simulation Results & Discussion

Mixed-mode 3D-TCAD simulations were carried out to study the effects of supply voltage in 28-nm dual- and triple-well SRAM designs. Fig. 4 shows the simulation setup. Since only n-channel transistors have different well structure (p-channel transistors will be in n-well for both designs), only transistors MN1 and MN2 were modeled in TCAD as shown in Fig. 4(b) and 4(c); compact models were used for transistors MP1 and MP2. Both the n-channel transistors were modeled in the same TCAD structure and the transistors were separated by the minimum distance allowed by the design rules. (The exact details of the SRAM layout used in this study are proprietary.) The layout of an SRAM cell can either separate the n-channel transistors (MN1 and MN2) with an n-well between them that contains the p-channel transistors (MP1 and MP2), or the layout can bring the n-channel transistors together, with the p-channel devices kept in separate wells [10]. The latter design has been shown to improve multi-cell upsets [10]. The simulation results presented here illustrate the effect of bit reversal for the case where the n-channel transistors are close together.

TCAD models were calibrated to match the commercial process design kit (PDK). The block of silicon used for simulations was 10 µm × 10 µm × 10 µm. The incident ions were modeled using a Gaussian radial profile with a characteristic 1/e radius of 50 nm and a Gaussian temporal profile with a characteristic time of 2 ps. As discussed in [6], it is the overall charge deposited that determines whether upset reversal occurs; the specific ion track profile does not influence the underlying mechanisms.

The circuit was simulated in an initial state with the output of inverter 1 (I1) HIGH and inverter 2 (I2) LOW, which results in transistors MN1 and MP2 being in the OFF state, and transistors MP1 and MN2 being in the ON state. The ion is incident on the drain region of transistor MN1. The output of I1 and I2 for an ion strike with an LET of 1 MeV-cm$^2$/mg for both dual-well and triple-well TCAD models at 1V and 0.5V operation are shown in Fig. 5(a) and 5(b) , respectively. At 1V, there is no upset-reversal in either dual-well or triple-well

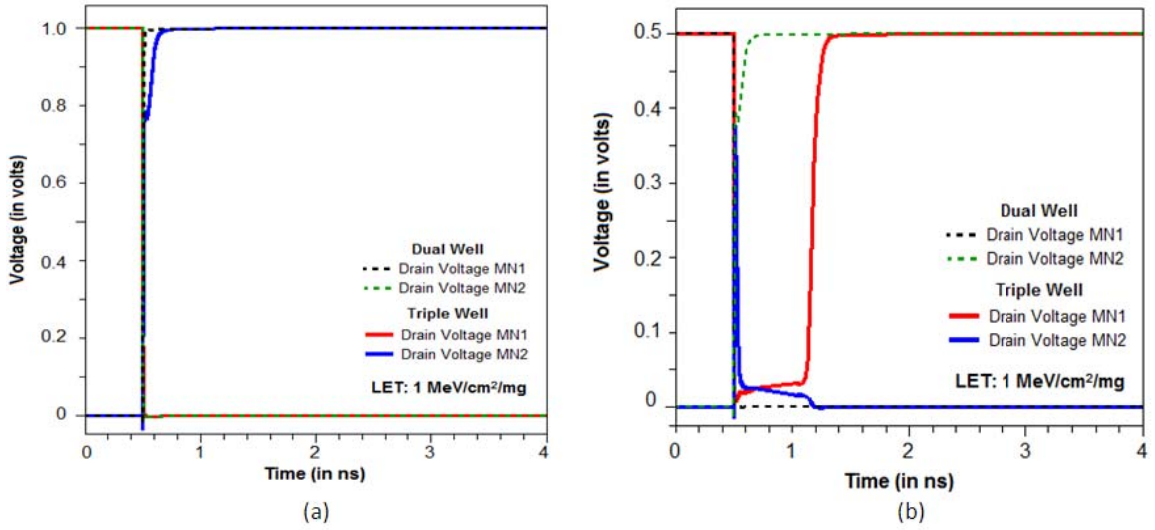


Fig. 5. Mixed-mode TCAD simulation results for LET = 1 MeV-cm$^2$/mg and for (a) Vdd = 1V showing no upset-reversal in either dual-well or triple-well designs (that is, the cell remains in flipped state) and for (b) Vdd = 0.5V showing upset-reversal occurring only in triple-well designs.

designs. However, for 0.5V operation the triple-well design shows an upset-reversal effect (that is, a recovery from the upset), while the output of the dual-well design remains upset.

As discussed in [6, 9], the mechanism of upset-reversal in triple-well designs is triggered by charge confinement in the p-well. In a triple-well structure, the deep n-well/p-well junction is reverse-biased. This causes the electrons to drift into the n-well, leaving behind holes in the p-well. In dual-well technology, the holes are spread throughout the p-substrate, while in triple-well technology the majority of the holes are confined within the p-well. This charge confinement in the p-well affects well voltage, and subsequently affects the operation of other transistors in the well. Initially, the transistor hit by the ion (MN1) is OFF, and when it collects charge, the output of inverter I1 changes. This turns the NMOS transistor (MN2) in the opposite inverter (I2) OFF, allowing it to collect charge that is still present in the p-well. If sufficient charge is collected by MN2, the cell reverts to its original state. The charge collected in the p-well is inversely proportional to the well doping [6]. Well doping increases with technology scaling, making the effect of charge confinement and subsequent bit-reversal less pronounced at nominal voltages for 28 nm technology [6]. However, at reduced supply voltages, the amount of charge needed is also lower, which bolsters the upset-reversal process and reduces the extent of MCUs.

The simulation discussion presented here is for the case where the n-channel transistors are in the same p-well. When the SRAM cell is designed with p-channel transistors in the same n-well and the n-channel transistors in separate p-wells, a similar type of bit reversal can occur for the p-channel transistors as discussed in [11]. More work is required to identify the differences in such bit reversal mechanisms between dual-well and triple-well designs. For example, while bit reversal for p-channel transistors may be similar for both dual and triple-well (since the p-channel transistors reside in an n-well in both cases), the impact of the deep n-well layer on the resistance of the well may also impact the well potential modulation and its extent as discussed in [12]. Additionally, in the case of the triple-well design, the n-channel transistors could still contribute to bit-reversal if charge gets deposited in both the p-wells containing the n-channel devices as discussed in the next paragraph. Thus the bit-reversal effect may still be dominant for the triple well design, especially at low voltages.

Based on previous works on ion track structures, the width of the initial track radius is generally larger than the minimum spacing distance between transistors in advanced technology nodes [13, 14]. In addition, M. P. King, et al. showed that delta-ray events are capable of depositing charge over many micrometers [15]. In an SRAM design at this technology node, even if the n-channel transistors are separated by an n-well, an ion hit may result in significant charge being deposited in both of the p-wells containing the n-channel transistors because the separation distance between the transistors is on the order of the initial track diameter. Furthermore, previous works have shown that an ion hit results in debiasing the well region (well collapse effect) because the deposited carrier concentration exceeds the doping concentration [16, 17]. This would result in a flow of charges across well boundaries in and around the strike location at the time of ion impact. Since the timescale of charge deposition and collection events are in the subnanosecond region, circuit-level effects begin to dominate rapidly, which can result in triggering the reinforcing charge collection mechanism, especially at low voltages. Hence the qualitative discussions presented in this work may still be applicable. Going forward, the extent and variation of the reinforcing charge collection must be modeled for different layout and spacing of transistors and across well boundaries.

## IV. CONCLUSIONS

This work presents the soft error response of dual-well and triple-well SRAMs over a range of supply voltages. Results for the 28-nm node show for the first time that triple-well designs are better suited to limiting the extent of MCU cross sections for alpha and heavy-ion particles at reduced supply voltages. Mixed-mode TCAD simulation results corroborate experimental results and show that the reinforced-charge collection (or upset-reversal) mechanism is responsible for reduced MCU SER at low supply voltages for triple-well designs. Low voltage operation is important for low power applications and for improving battery life during device standby mode. These results indicate that commercial designs targeted for very low voltage and subthreshold voltage operation can benefit from the triple-well option, while the dual-well option has the advantage for nominal voltage operation.

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