# Figure of Merit for Selecting Super-Junction MOSFETs in High Efficiency Voltage Source Converters

Andrew Hopkins, Neville McNeill, Philip Anthony, Phil Mellor
Department of Electrical and Electronic Engineering,
University of Bristol,
Bristol, England
e-mail: Andrew.Hopkins@bristol.ac.uk

***Abstract*— Silicon super-junction MOSFETs have very low on-state resistances and fast switching characteristics. However, their use in voltage-source converters is hindered by the poor reverse recovery performance of their body drain diode and an adverse output capacitance characteristic. These both act to increase the overall switching loss. The on-state resistance and output capacitance characteristics of super junction devices are both related to the area of the silicon die. As this increases, the on-state resistance decreases but the output capacitance increases. A figure of merit is evaluated with both predicted and experimental results using a 400-V, DC-DC synchronous buck-converter operating over a range of output currents and switching frequencies.**

## I. INTRODUCTION

The vertical structure of super junction (SJ) MOSFETs [1], [2] differs from that of the more conventional planar variants in such a way that SJ devices exhibit a significantly higher blocking voltage capability and reduced on-state resistance for the same die area. The benefits this technology offers are achieved at an acceptable cost and mean SJ devices are now being considered as an alternative to IGBTs and SiC MOSFETs at voltage levels above 200 V.

However, the P-columns in SJ devices cause the output capacitance ($C_{oss}$) to be extremely non-linear and its magnitude to be far greater than that of a planar MOSFET. This $C_{oss}$ characteristic, along with the poor reverse recovery performance of the intrinsic anti parallel diode, makes their deployment in voltage-source converter (VSC) applications difficult. Several techniques are available for intrinsic diode deactivation [3]. However, even if effective intrinsic diode deactivation is implemented, it is necessary to address the $C_{oss}$ characteristic in VSC applications. Most of the stored charge, $Q_{oss}$, in $C_{oss}$ is sourced at a low drain-source voltage. A large current transient is experienced by the complementary incoming forward device in a bridge leg, which causes undue stresses on this device as well as EMI difficulties. A linear inductive snubber circuit [4] can be used to control this current. With the addition of a secondary winding to the inductor, a proportion of the energy drawn from the supply rail to supply $Q_{oss}$ can be actively recovered with a SMPS. Whilst adding complexity, the result is a highly efficient (>99%) power converter stage with the major benefits of reduced heatsinking and compactness.

Both the on-state resistance and output capacitance are directly related to the area of the silicon die. Thus the device which achieves the least losses, in a given circuit, is not necessarily that which has the lowest on-state resistance, due to the losses related to $C_{oss}$. There are three main figure of merits (FOMs) which can be used to inform silicon MOSFET selection. These include the $Q_G$ FOM [5], [6] (minimizes gate charge loss for a given $R_{DS(on)}$), the $Q_{GD}$ FOM [7] (minimizes control MOSFET switching losses for a given $R_{DS(on)}$) and the $Q_{oss}$ FOM [8] (minimizes output capacitance loss for a given $R_{DS(on)}$).

The FOM in [8] is often applied in device selection for high frequency applications using planar MOSFETs. The output capacitance characteristic of these devices is significantly more linear and the output capacitance is shown to scale with the square of the drain voltage. This is not the case with SJ MOSFETs as the $C_{oss}$ is highly non-linear and typically the majority of the charge is supplied when the drain voltage is below 50 V after which there is comparatively little additional charge drawn up to the device's maximum blocking voltage. Furthermore the magnitude of its $C_{oss}$ is significantly larger than in a planar device. The losses associated with charging and discharging this capacitance are significant at the multiple hundreds of volts level. In a VSC, the rail voltage affects the charging rate and can be managed via switching aid circuitry [4]. However even with reactive components (inductors) and deactivation of the intrinsic body-drain diode, these additional components are inevitably not ideal and losses are incurred. In comparison, the losses associated with the gate or gate to drain charges are considerably smaller. In this paper, the $Q_{oss}$ FOM is re-evaluated and proposed as the

978-1-4673-7151-3/15/$31.00 ©2015 IEEE

most appropriate technique for selecting SJ MOSFETs in high efficiency VSCs.

## II. THE PROPOSED FIGURE OF MERIT

The bidirectional DC-DC converter topology in Fig. 1 is used to investigate the non-linear $C_{oss}$ variation and the proposed FOM. At any point in time one of the two switches conducts and the other is off, ignoring any dead-times. The conduction losses, $W_c$, for the circuit are therefore calculated using:

$$W_c = I^2 R_{DS(on)} \tag{1}$$

where $I$ is the RMS load current and $R_{DS(on)}$ is the device's on-state resistance. The effective duty cycle for this circuit is one due to current always flowing through one device at any given time. On the other hand, in an AC to DC or DC to AC converter a duty cycle of two must be included as the current normally always flows through two devices.

The $C_{oss}$ of an SJ MOSFET is extremely non-linear. The Engauge Digitiser [9] program was used to capture the $QV$ curves from the manufacturers' capacitance graphs. This allows the charge stored in $C_{oss}$ to be calculated. Fig. 2 shows the $QV$ curve obtained in this way for the Infineon CoolMOS IPW60R041C6 device [10].

The shaded area above the curve represents the energy stored in $C_{oss}$. The energy below the curve represents the energy drawn from the supply rail in the course of charging $C_{oss}$. The energy stored in a linear capacitor, $E_{lin}$, is given by:

$$E_{lin} = \frac{1}{2} QV \tag{2}$$

where $Q$ is the charge and $V$ is the applied voltage. It is seen that the stored energy is significantly lower for $C_{oss}$ due to its non-linearity. This is advantageous in single-ended applications where self-discharge losses are consequently low.

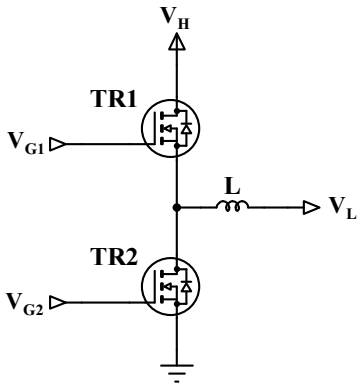


Figure 1. Bidirectional half bridge converter topology.

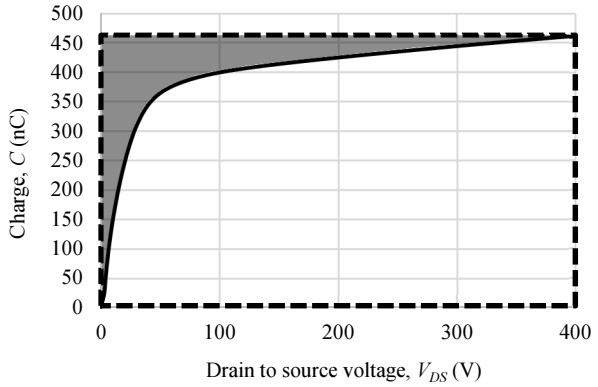


Figure 2. $QV$ characteristic for an Infineon IPW60R041C6 CoolMOS MOSFET [10].

The area under the curve can be approximated as rectangular, depicted by the dotted line in Fig. 2. Typically, the error in neglecting the stored energy path (the shaded area) will be less than 20%. The energy, $E$, represented by this area is given by:

$$E = Q_{oss} V \tag{3}$$

From (3), the switching-associated losses, $W_s$, were calculated using (4):

$$W_s = fE \tag{4}$$

where $f$ is the switching frequency. Inserting the result from (3) into (4) gives:

$$W_s = fQ_{oss} V \tag{5}$$

If an energy recovery technique with an efficiency, $\eta$, is used, instead of supplying $Q_{oss}$ dissipatively, (5) can be rewritten as (6):

$$W_s = fQ_{oss} V(1-\eta) \tag{6}$$

The conduction losses, $W_c$, and $C_{oss}$-associated switching losses, $W_s$, are the most significant in this circuit. If intrinsic diode reverse recovery losses are eliminated with a deactivation technique and the driver losses are neglected, the total losses, $W_T$, can therefore be calculated using:

$$W_T = I^2 R_{DS(on)} + fQ_{oss} V(1-\eta) \tag{7}$$

A figure of merit, $F_M$, can be defined by:

$$F_M = R_{DS(on)} Q_{oss} \tag{8}$$

This is determined from the relationship a device's $R_{DS(on)}$ and $C_{oss}$ has with its silicon die area. Devices with a smaller $R_{DS(on)}$ are constructed using a larger area of silicon. However the $C_{oss}$ of a device increases with the area of silicon used. Rearranging (8) in terms of $Q_{oss}$ gives (9):

$$Q_{oss} = \frac{F_M}{R_{DS(on)}} \tag{9}$$

(7) can be rewritten with the insertion of the result from (9) to give:

$$W_T = I^2 R_{ds(on)} + f \frac{F_M}{R_{DS(on)}} V(1-\eta) \tag{10}$$

Fig. 3 shows that the point of minimum losses does not necessarily coincide with the lowest value of $R_{DS(on)}$. Differentiating (10) gives the optimum $R_{DS(on)}$ at which this point of minimum losses would be achieved. This figure of merit can also be applied in the case of a generic H-bridge converter. However the effective duty cycle of the circuit will be two as the conduction losses are double that of a buck converter, due to two devices conducting at any one instant in time. The applicable loss equation for the H-bridge converter is:

$$W_T = 2I^2 R_{ds(on)} + f \frac{F_M}{R_{DS(on)}} V(1-\eta) \tag{11}$$

## III. Experimental Hardware

A single phase-leg from the circuit in [4], Fig. 4, was used to obtain experimental results to evaluate the proposed figure of merit. $V_H$ was 400 V. TR1a and TR2a are auxiliary low-voltage MOSFETs (Infineon IPD031N03L G [11]), used to deactivate the intrinsic diodes in the main MOSFETs, TR1 and TR2 [3]. The deactivation circuit for TR1 (R2, D1, TR1a and D2) is only required when the single phase-leg operates as a boost converter. The circuit was operated solely as a buck converter for the experimentation in this paper, thus these components are only shown for completeness. $L_s$ is a linear snubber inductor used to control the $C_{oss}$ charging currents into TR1 or TR2, depending on the direction of power flow. It was based around a Micrometals T80-8/90 toroidal core with N = 16. The inductance was taken as 4.89 µH from measurements in [4]. TR1 and TR2 were mounted onto a heatsink, which had a measured thermal resistance, Rth, of 6.6°C/W. This was determined by means of a thermal superposition test;

$$R_{th} = \frac{\Delta T}{W} \tag{12}$$

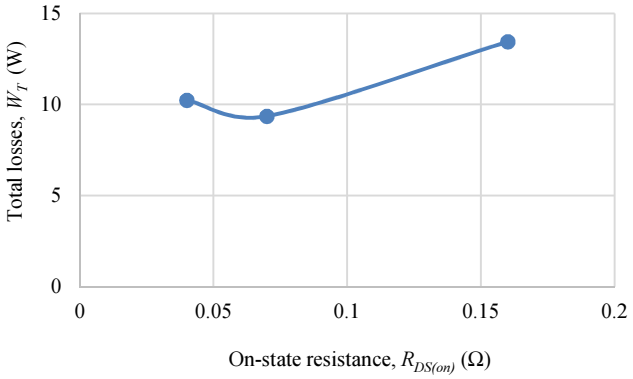


Figure 3. Exemplifying curve of $W_T$ against $R_{DS(on)}$ for a current of 6 A, switching frequency of 40 kHz and a rail voltage of 400 V.

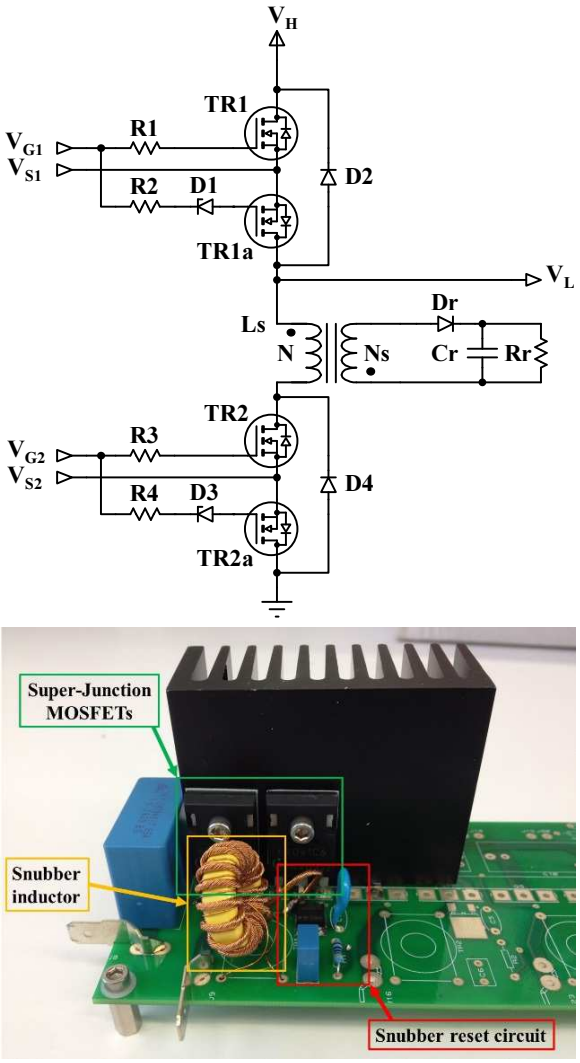


Figure 4. Top: Schematic diagram of experimental circuit showing inductive snubber and reset circuit [4]. Bottom: Photograph of experimental hardware.

where $W$ is a known DC power dissipated in the devices on the heatsink and $\Delta T$ is the temperature increase above ambient. Once the heatsink reached thermal equilibrium $R_{th}$ could be calculated. The power dissipated when testing under actual switching conditions can subsequently be calculated from the temperature measurement recorded above ambient once $R_{th}$ is known.

Energy is recovered from $L_s$ by means of a recovery winding, Ns. This energy was dissipated in the resistance, Rr. The power could then be calculated to find the $C_{oss}$-related switching loss incurred by TR2's output capacitance. In [4] an SMPS returns energy to the supply rail, but a resistive reset circuit is used here for experimental purposes.

Once this power is added to the losses dissipated into the heatsink, the total losses for the switching devices under test could be obtained. The devices were tested at the current levels: 4 A, 5 A and 6 A and at the switching frequencies: 5 kHz, 20 kHz, 30 kHz and 40 kHz. Although these currents are well below the MOSFETs' rated values, considerable gains in efficiency are possible at these ratios of actual to rated current when compared with IGBT-based circuits [4], [12]. These current levels were selected to compare the $R_{DS(on)}$ conduction losses against the $C_{oss}$-related losses. Increasing the current increases each device's offset from the x-axis as shown in the results (determined by the $R_{DS(on)}$ of the device). In selecting a heatsink with a target $R_{th}$ value, a compromise was reached between an excessive $\Delta T$ causing inaccuracies between the results of each device due to the effect temperature has on the $R_{DS(on)}$, yet giving a reasonable heatsink temperature rise for all three devices and a good degree of resolution in the results.

The load was selected so that the duty cycle, $\delta$, could be low (<20%) for all three current levels. A low $\delta$ keeps the majority of conduction losses in the bottom device in the bridge leg. For convenience, the top device was unchanged throughout the experimentation (Infineon IPW60R041C6 [10]). The $C_{oss}$-related losses are only incurred by the bottom device. Thus the switching losses and conduction losses are principally dependent on the device under test, namely the bottom device. As a low-$R_{DS(on)}$ device was used in the top position the effect of slight variations in the duty cycle between the three devices under test, which were used to maintain the same current for all of the devices, is reduced. The losses in the top device are therefore similar for all three devices, reducing the variation in the heatsink temperature. Maintaining a constant loss in this device, as much as possible, reduces the additional heatsink rise in temperature. This would have a knock on effect on the bottom device by increasing the device's $R_{DS(on)}$, leading to inaccurate results.

The diode-resistor combinations, D1-R2 and D3-R3, are included to ensure the auxiliary MOSFETs switch off before the main SJ-MOSFETs. This is important as it deactivates the intrinsic diode of the SJ-MOSFET which has extremely poor reverse recovery behavior. A 1N4729A Zener diode [13] with a Zener voltage of 3.6 V was selected. The threshold voltage of the auxiliary MOSFET can be as low as

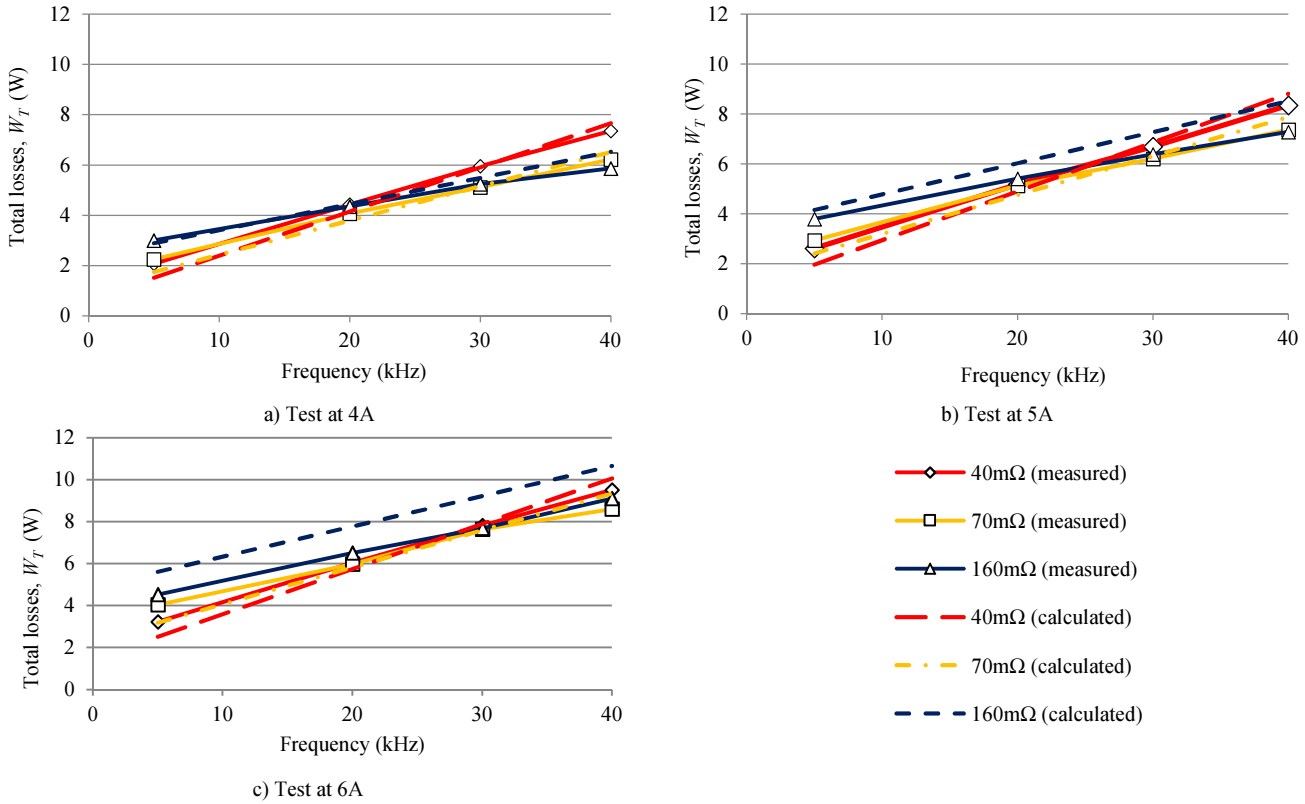


Figure 5. Calculated (dotted) and measured (solid) aggregate heatsink and inductive snubber reset circuit losses for the three devices at 4 A, 5 A, and 6 A over the selected range of frequencies (60% energy recovery was assumed for all of the results). The results are for the DC-DC converter configuration.

1 V. This is approximately 3.2 V lower than the SJ MOSFET gate threshold voltage. Without this diode the main device will switch off before the auxiliary MOSFET and thus allow its intrinsic diode to conduct. Circuit losses would consequently increase due to the reverse recovery charge which must be supplied to the now forward biased body drain diode of the synchronous rectifier SJ-MOSFET.

The DC-DC converter results are shown in Fig. 5 along with the calculated losses. The calculated losses are the total losses attributed to the conduction and $C_{oss}$-related switching losses, assuming a conservative energy recovery efficiency of 60%, as given in (10). In addition to these loss mechanisms; other smaller losses were included for accuracy in the calculated losses. These were switching and self-discharge losses, and snubber inductor-related switching losses. It is noted that some losses in $L_s$ and Dr are incurred.

The conduction losses were calculated using the value of $R_{DS(on)}$, provided by the manufacturers. The FOM introduced in (8) was found to only vary marginally between all of the SJ MOSFETs that were assessed. Additionally, this trend was observed across devices from a number of different manufacturers. This is due to the relationship between a SJ MOSFETs' $R_{DS(on)}$ and its $Q_{oss}$. An approximate value of $F_M$ for a 600-V rated device is 21 nΩC. Using (5) and the $QV$ data obtained from the capacitance curves of the three devices selected (41-mΩ, 70-mΩ and 160-mΩ devices from the C6 family in the T0247 package type), the $C_{oss}$-related switching losses were calculated. $C_{oss}$ and $R_{DS(on)}$ are linked with the $F_M$ previously determined. Turn-on and turn-off switching intervals were both taken as 50 ns for calculation of the switching losses. The self-discharge loss was determined by multiplying $f$ and the manufacturer's value of self-discharge energy $E_{oss}$. The snubber inductor-related switching loss, $W_2$, which is caused by the transfer of energy through $L_s$ when current is initially forced into it, was calculated using:

$$W_2 = \frac{f L_s I_{LOAD}^2}{2} \tag{13}$$

The measured losses are the aggregate heatsink and snubber circuit reset losses, where the dump resistor losses are multiplied by a factor of 0.4 to match the energy recovery

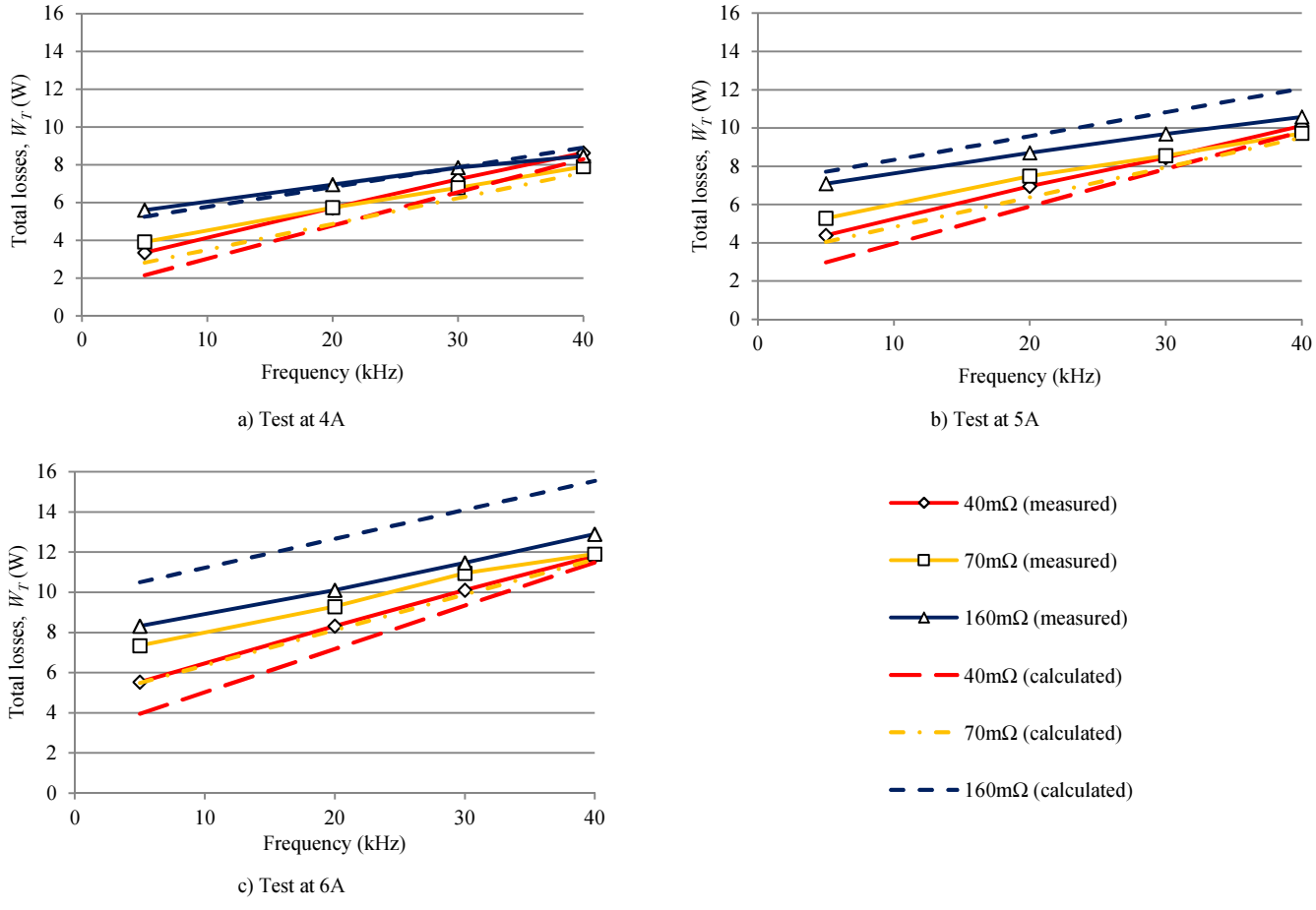


Figure 6. Calculated (dotted) and adjusted (solid) aggregate heatsink and inductive snubber reset circuit losses for the three devices in an inverter configuration. Each device was measured at 4 A, 5 A, and 6 A over the selected range of frequencies (60% energy recovery was assumed for all of the results).

efficiency applied to the calculated losses.

The heatsink temperature was measured over a period of 60 minutes or until at least two successive results were recorded to be the same. The same spot was used on the heatsink for each of the measurements to maintain accuracy and repeatability. The ambient temperature was measured using an aluminum block placed in the same enclosure as the circuit. This was done to minimize variations due to local air currents. The temperature was recorded at the same time as the heatsink measurement was taken. The temperature rise above ambient of the heatsink was then calculated using these two figures. The power dissipation into the heatsink could then be found using (12), and the known value of $R_{th}$ previously calculated.

The graphs in Fig. 5 show cross-over points where the most appropriate device changes. As expected, at low currents and the highest tested switching frequencies, the device with the largest $R_{DS(on)}$ outperforms the device with the lowest $R_{DS(on)}$. For each of the current levels assessed, the gradient of the graphs decreases as the device's $R_{DS(on)}$ increases. At higher currents the cross over point is shifted to higher frequencies. This is due to the relationship between a device's $R_{DS(on)}$ and its $Q_{oss}$ supporting the new FOM discussed in this paper. It is noted that ideal intrinsic diode deactivation is assumed here. The gradient of the lines for each device are essentially constant due to the switching-associated loss dependence on frequency. As expected, the gradients are found not to vary proportionally with current level, as the dominant loss is not the traditional switching loss, but is the loss given by (6), which is independent of current. However, it is noted that there is a smaller component dependent on the current squared, given by (13).

Fig. 6 shows inferred results for when the devices are used in an inverter. As discussed previously, the conduction losses are double that of those in a DC-DC converter. The calculated losses were recalculated using (11). The measured losses were also adjusted. The proportion of loss made up by the conduction losses for the DC-DC converter was determined from the previously measured results. Finding the equation for these results and calculating the y-axis intercept point gives an accurate representation of the conduction losses. Thus multiplying this by a factor of two gave a close approximation for the quantity of conduction losses which would be expected in an inverter application.

The 160-mΩ MOSFET's losses do not cross over those of the lower-$R_{DS(on)}$ devices until higher switching frequencies. Due to the additional conduction losses, when the current level increases this cross-over point shifts to higher frequencies than in the DC-DC converter results shown in Fig. 5. The selection of SJ MOSFETs with higher $R_{DS(on)}$ values for inverter applications is therefore more dependent on the load current. However, as seen in Fig. 5, the 70-mΩ device has lower losses at high frequencies than the 40-mΩ device. Choosing a higher-$R_{DS(on)}$ device will normally result in lower cost as well as the improved power stage efficiencies above the cross over point, for a given load current.

## IV. Conclusion

A figure of merit has been presented which addresses SJ MOSFET selection for voltage source converters. The device, which achieves the least losses, has been shown to vary depending on the switching frequency and current level in a circuit. The proposed figure of merit theory is shown to be supported by the results. The effect of deploying SJ devices in an inverter application has been compared with the losses experienced when they are used in a DC-DC converter.

## V. Acknowledgment

The authors gratefully acknowledge the financial support of the UK Engineering and Physical Sciences Research Council (www.epsrc.ac.uk, Grant No. EP/I031707/1, Vehicle Electrical Systems Integration (VESI)).

## VI. References

[1] J.-S. Lai, B.-M. Song, R. Zhou, A. Hefner, Jr., D. W. Berning, and C.-C. Shen, "Characteristics and utilization of a new class of low on-resistance MOS-gated power device", IEEE Transactions on Industry Applications, Vol. 37, No. 5, pp. 1282-1289, September/October 2001.

[2] L. Lorenz, G. Deboy, and I. Zverev, "Matched Pair of Coolmos Transistor with SiC-Schottky Diode - Advantages in Application", IEEE Transactions on Industry Applications, Vol. 40, No. 5, pp. 1265-1272, September 2004.

[3] D. B. DeWitt, C. D. Brown, and S. M. Robertson, "System and Method for Reducing Body Diode Conduction", US Patent No. 7508175 (B2), 24 March 2009.

[4] N. McNeill, P. Anthony, and N. Oswald, "Ultra-high efficiency machine drive inverter using super-junction MOSFETs", Proceedings, 7th IET Power Electronics, Machines and Drives Conference (PEMD 2014), Manchester, UK, April 2014.

[5] B. Jayant Baliga, "Power semiconductor device figure of merit for high-frequency applications," IEEE Electron Device Letters, Vol. 10, No. 10, pp. 455-457, October 1989.

[6] D. Cucak, M. Vasić, O. Garcia, J. Oliver, P. Alou, and J. Cobos, "Optimum design of an envelope tracking buck converter for RFPA using GaN HEMTs," Proceedings, 3rd IEEE Energy Conversion Congress and Exposition (ECCE2011), Phoenix, AZ, USA , pp. 1210-1216, September 2011.

[7] A. Q. Huang, "New unipolar switching power device figures of merit", IEEE Electron Device Letters, Vol. 25, No. 5, pp. 298-301, May 2004.

[8] I.-J. Il-Jung Kim, S. Matsumoto, T. Sakai, and T. Yachi, "New power device figure-of-merit for high frequency applications," Proceedings, 7th International Symposium Power Semiconductor Devices and ICs, pp. 309-314, Yokohama, Japan, May 1995.

[9] Engauge digitiser program version 5.1 [Online], available: digitizer.sourceforge.net, accessed December 2014.

[10] IPW60R041C6 Datasheet [Online], available: www.infineon.com, accessed December 2014.

[11] IPD031N03L G Datasheet [Online], available: www.infineon.com, accessed June 2015.

[12] J. Kimball and P. Chapman, "Evaluating conduction loss of a parallel IGBT-MOSFET combination," Conference Record, 39th Industry Applications Conference, Vol. 2, pp. 1233-1237, Seattle, WA, USA, October 2004.

[13] 1N4729A Datasheet [Online], available: www.fairchildsemi.com, accessed June 2015.