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Operating Channel Temperature in GaN HEMTs: DC versus RF Accelerated Life Testing

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Abstract— **Channel temperature is a key parameter for accelerated life testing in GaN HEMTs. It is assumed that self-heating is similar in RF and DC operation and that DC test results can be applied to RF operation. We investigate whether this assumption is valid by using an experimentally calibrated, combined electrical and thermal model to simulate Joule heating during RF operation and compare this to DC self-heating at same power dissipation. Two cases are examined and the implications for accelerated life testing are discussed: Typical (30 V) and high (100 V) drain voltages.**

Keywords- GaN, HEMT, reliability, temperature, simulation, thermography, RF.

I. INTRODUCTION

Accelerated life tests are required to ensure the long term reliability of emerging technologies including AlGaN/GaN HEMT based RF power amplifiers. Channel temperature data is a critical parameter for high temperature operating life (HTOL) tests. Measurements performed at multiple junction temperatures enable activation energies to be determined by applying the Arrhenius equation [1]. Mean time to failure (MTTF) can then be extrapolated from the elevated test temperature to the normal operating temperature, typically around 175°C for GaN devices. Such a test would ideally be undertaken using the actual operating condition for the device under test (DUT) application, e.g. RF operation for a GaN RF amplifier. However, the cost and complexity of RF-HTOL testing means that the number of devices tested is more limited than for DC-HTOL, leading to a larger statistical uncertainty in the results obtained. Typically an MTTF determined from DC-HTOL test will be applied to predict the lifetime of devices during RF operation, verified by performing RF life tests on a reduced number of DUTs.

The channel temperature increase during operation is the result of Joule self-heating, which is the scalar product of electric field and current density (J•E) in the transistor channel. Self heating is influenced by the drain and gate bias voltage [2], and as a consequence the Joule heating power dissipation profile in the channel will vary during RF operation. This raises the question, is the channel temperature equivalent during RF and DC operation, even when channel power dissipation is carefully matched? This question is particularly relevant when GaN HEMTs are operated at higher than typical drain voltages, which can be advantageous for high power applications.

A large temperature gradient is generated in AlGaN/GaN HEMTs during operation, owing to the highly localized power dissipation density in the channel coupled with the relatively efficient heat extraction through the GaN layer and substrate. Consequently, measuring the peak channel temperature directly can be very challenging owing to the finite spatial resolution of experimental thermography techniques. IR thermography or electrical methods average temperature over a much larger area than the power dissipation region in the HEMT channel, introducing uncertainty when relating the measured temperature to the actual channel temperature [3]. Raman thermography, a laser scattering based microscopy technique, was developed to enable measurements closer to the peak channel temperature location [4,5], having a lateral spatial resolution of around 0.5 µm. Despite this improved optical resolution, GaN HEMT temperatures measured using Raman thermography are lower than the peak channel temperature. Therefore, thermal modeling calibrated by measurement is needed to determine the actual channel temperature – which is the parameter needed for HTOL tests.

Device thermal models require accurate knowledge of both the material thermal properties and the power dissipation profile within the device channel. Material parameters can be verified by measurement (e.g. fitting simulation to measurement), whereas drift diffusion simulations are needed to determine the exact power dissipation profile in the channel at the measurement condition used. At low drain bias voltages, the Joule heating region can be approximated as 0.5 µm-long block heater located close to the gate foot [5]. Field plates are designed to spread the electric field at higher drain voltages, protecting the gate. Consequently, Joule heating also spreads away from the gate as the drain voltage is increased [2]. During RF operation the gate and source-drain voltage will vary continuously along a load line and at each bias point the power dissipation profile in the channel will be different. This may result in a difference between the RF and DC channel temperature profile and peak temperature during operation, even if the channel power dissipation is the same.

As described previously, it is not currently possible to measure the channel temperature profile directly. We have developed a combined electrical and thermal device model to evaluate the channel temperature, using 2D drift diffusion (Joule heating) and 3D finite element (thermal), calibrated using Raman thermography measurements. We consider self-

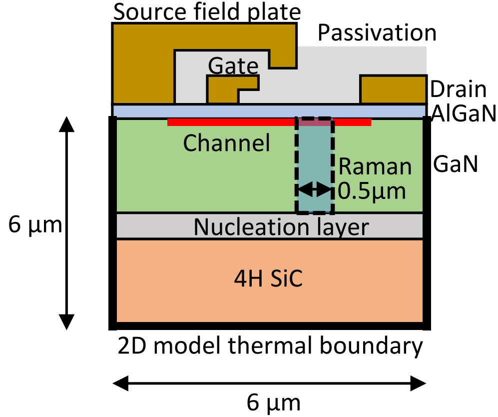

Figure 1: Schematic cross section of the AlGaN/GaN HEMT gate finger, showing the area in the GaN layer measured by Raman thermography with respect to the channel were Joule heating occurs. The external dimensions indicate the size of the 2D drift diffusion simulation cell and the bold line represents a thermal boundary conductance used to approximate the device thermal resistance.

heating during RF and DC operation at two drain bias voltages: 30V, which is a representative value for this technology and 100V, which is an extreme value to illustrate the possible differences between DC and RF self heating. The potential implications for HTOL testing are discussed.

II. Experimental Details

Eight finger AlGaN/GaN HEMTs with a width of 125 µm (1mm total gate periphery) were tested and modeled. The epitaxy consisted of an AlGaN barrier, GaN buffer, AlN nucleation layer and 100 µm-thick SiC substrate [6]. The gate finger cross section is illustrated schematically in Fig. 1, consisting of a 0.25 µm gate, gate field plate, source terminated field plate and a 2.7 µm gate-drain spacing. The device die was soldered onto a Cu carrier using AuSn eutectic. A thermoelectric chuck was used to maintain the temperature of the metal carrier back side at 25 ºC during measurements, monitored by a thermocouple. Electrical contact was made using G-S-G probes and 50-Ohm terminated bias-T's to ensure stable DC operation during thermal measurements.

Micro-Raman thermography measurements were performed for comparison to the thermal model results. The temperature of the GaN layer was derived from the measured GaN A_1(LO) phonon shift: Further details about the Raman thermography technique can be found in [3,4,5]. Figure 1 illustrates the temperature measurement location, which is 0.5 µm from the drain edge of the field plate. An 0.5 numerical aperture objective was used for light focusing and collection, achieving a lateral spatial resolution of 0.5 µm. The GaN layer is transparent at the 532 nm laser wavelength used and therefore the measured GaN temperature represents a depth average through the GaN layer. An addition temperature point measured close to the corner of the die was used to evaluate the thermal resistance between the die and carrier.

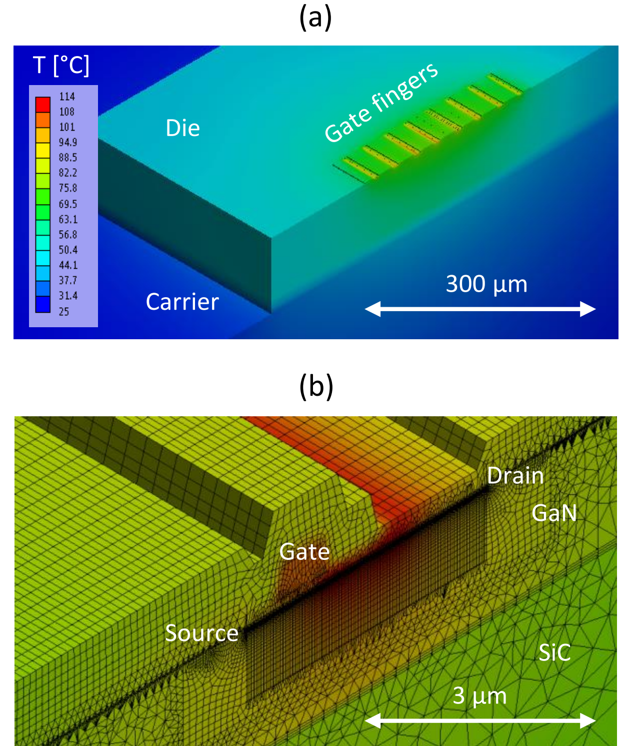

Figure 2: Surface temperature plots showing a symmetric ½ of the 8 finger HEMT mode with a power dissipation of 5.9 W/mm at an ambient temperature of 25 °C: (a) Overview showing gate fingers, die and a portion of the carrier; (b) Cross section of one gate finger in the finite element thermal model, including the mesh. A 1 nm node spacing is used in the GaN layer close to the channel enabling Joule heating distributions to be input directly from a drift diffusion simulation. The entire 8 finger HEMT model, including die and carrier, consists of ~3 million elements; The model can also be applied to transient simulations, e.g. a 1 ms duration pulse simulation can be solved in 20-30 minutes using a desktop computer.

III. Model

It is possible to model channel temperatures using a fully coupled electrothermal drift diffusion model [2], although simplified thermal boundary conditions are used to reduce their computational complexity. For example, the typical simulation cells are two dimensional and restricted in size. Figure 1 shows a schematic illustration of the 6×6 µm 2D drift diffusion model cell, representing a gate finger of the measured HEMT. A thermal boundary conductance is introduced between the edge of the semiconductor in the simulation cell, indicated in Fig. 1, and an isothermal boundary set to the experimental chuck temperature; this boundary condition approximates the total thermal resistance between the gate finger and the thermal chuck. The thermal conductance is adjusted to approximately match the measured temperature. Since thermal resistance is temperature and layout dependent, the 2D model alone has limited accuracy when predicting channel temperature when the temperature is changed or device geometry is varied, e.g., the effect of gate pitch or width on thermal cross talk. The simple thermal boundary conductance used also does not include the heat capacity of the device outside the simulation

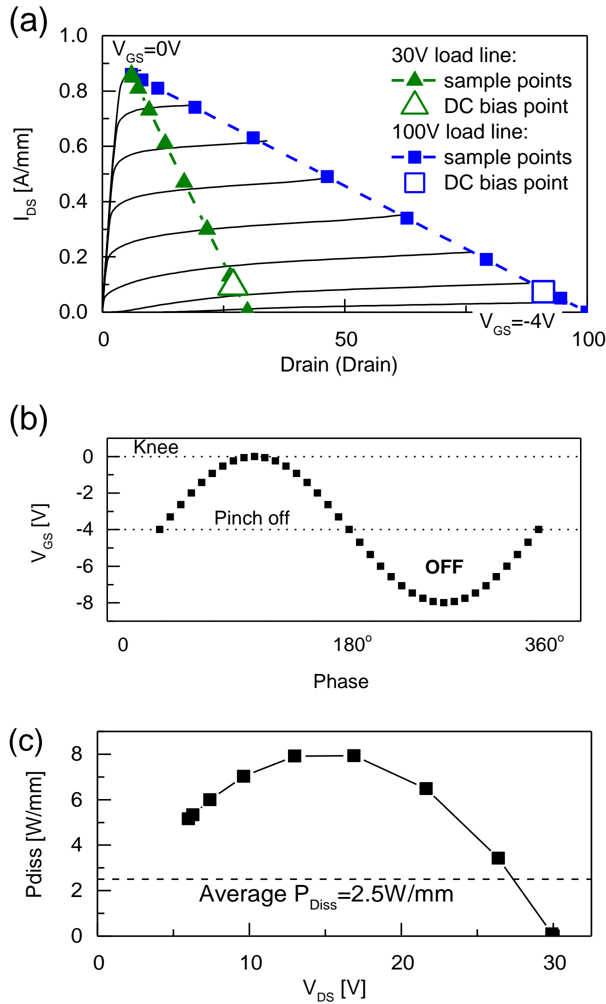

Figure 3: (a) HEMT IV characteristics simulated using a drift diffusion model, matching the measured IV characteristics. Class B load lines at a drain voltage of 30V and 100V are overlaid. (b) A sinusoidal gate voltage with uniform time steps is used to generate sample points on the load lines shown in (a). The Joule heating distribution in the HEMT channel is calculated at each of the points shown. (c) Power dissipation in the HEMT channel as a function of drain voltage along the load line, e.g. shown for the 30V load line. The horizontal line indicates the power dissipation averaged over the load line, used to select the equivalent P_{diss} bias point shown in (a).

cell, so cannot be used to accurately predict temperatures during pulsed operation.

Alternatively, finite element (FE) thermal modelling can be used to determine channel temperature. FE has the advantage that detailed models can be computed, accurately representing the geometry of large devices. The drawback of the FE approach is that power dissipation profile in the channel is typically input manually and is approximate. At low drain voltages a block heater adjacent to the drain edge of the gate can be used to approximate the high field region, although this is not valid at higher drain voltages in transistors with field plates [2]. In this study we have implement a combined approach, including the benefits of a 2D drift diffusion model

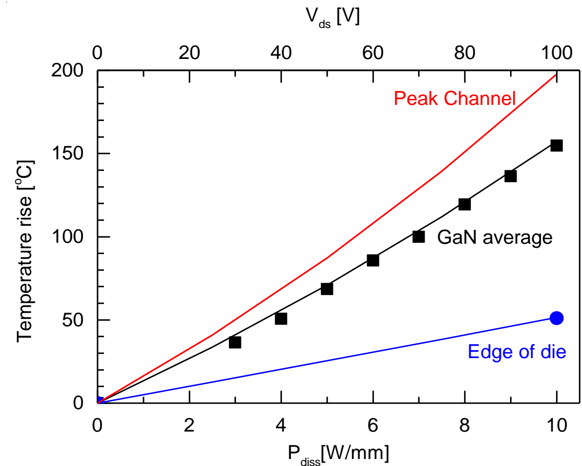

Figure 4: Raman thermography results measured at a 100 mA/mm drain current and varying drain bias. Transistor and corner of die temperatures (symbols) measured by Raman thermography. The measured transistor temperature is averaged through the GaN layer, as illustrated in Fig. 1. Simulated temperatures (solid lines) are overlaid on the measurement data for comparison, including the peak channel temperature.

and a 3D FE model: The 2D drift diffusion model is used to calculate the Joule heating distribution, which is then input into the 3D FE model for improved temperature accuracy, including the complete device and carrier. We note that unlike a fully coupled electrothermal model, the electrothermal interaction is lost when the power dissipation profile is transferred to the FE model. The implications of this for the accuracy of the predicted of channel temperatures will be discussed.

Silvaco Atlas was used to perform the 2D drift diffusion simulations, adapting the model described in [7,8]. Model parameters, including the polarization charge at the GaN/AlGaN interface and GaN mobility, were adjusted to match the measured transconductance, pinch-off voltage and saturated drain current. The FE model was implemented in ANSYS, accurately reproducing the gate finger geometry, layout, die and carrier. Particular attention was given to meshing the GaN channel, shown Fig. 2(b), enabling the 2D Joule heating map obtained in Silvaco Atlas to be used as an input: To do this the simulated 2D heat map was extruded into 3D heat generation volume and applied to each gate finger by interpolation onto the FE model nodes, matching the total power dissipation in the model to the measured power dissipation in the device. The thermal conductivity values reported in previous work were used [4], including a GaN thermal conductivity of 160 W/mK ($T^{-1.4}$ temperature dependence) and SiC thermal conductivity of 420 W/mK ($T^{-1.1}$ temperature dependence). Two parameters were adjusted in the model to fit the measured temperatures: the die attach layer thermal resistance and the effective thermal boundary resistance (TBR_{EFF}) at the interface between the GaN and SiC layers. Both these parameters need to be obtained from measurement since they can be affected by the fabrication process and epitaxial growth conditions. The die solder thermal conductivity was adjusted to fit the measured temperature at

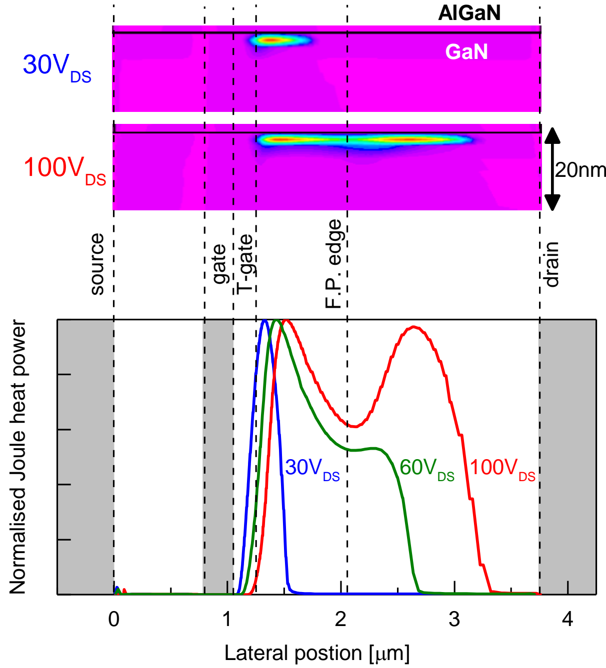

Figure 5: Simulated Joule heat power distributions in the HEMT channel in the semi-on condition, at a drain current of 100 mA/mm. The upper plots show the 2D joule heat power distribution in the channel in cross section through the HEMT channel at $30V_{DS}$ and $100V_{DS}$. The aspect ratio has been exaggerated for visual clarity, showing an area of 3.75µm×0.02µm. The lower plot shows normalized lateral Joule heat power distributions at a depth of 1 nm below the AlGaN/GaN interface.

the corner of the die. The TBR_{eff} value used is 0.8×10^{-8} m^2K/W at 25°C, with a $T^{0.9}$ temperature dependence, which lies within the range of reported values for different wafer vendors [9]. An isothermal boundary condition was applied to the back side of the carrier in the model, matching the chuck temperature used during the device measurements. All other external surfaces in the model have an adiabatic boundary condition. The resulting 3D temperature distribution across the surface of the die is illustrated in Fig. 2(a).

The modelling approach described here enables the channel temperature to be obtained from the FE model at any bias point in the IV plane without making assumptions about the power dissipation profile. To investigate channel heating during RF operation, when voltage and current varies continuously along a load line, the channel power dissipation profile must be simulated at multiple points in the IV plane. Figure 3(a) shows the simulated IV characteristics of the HEMT, matching the measured IV characteristics. For RF operation we consider class-B operation which is typical for GaN high power amplifier applications, although this analysis could equally be performed for any other operating class. Two load lines are considered, at a drain voltage of 30V and 100V, overlaid onto the simulated IV curves in Fig. 3(a). For this analysis we are using a low frequency load line, represented as a straight line in the IV plane. Although the load line deviates

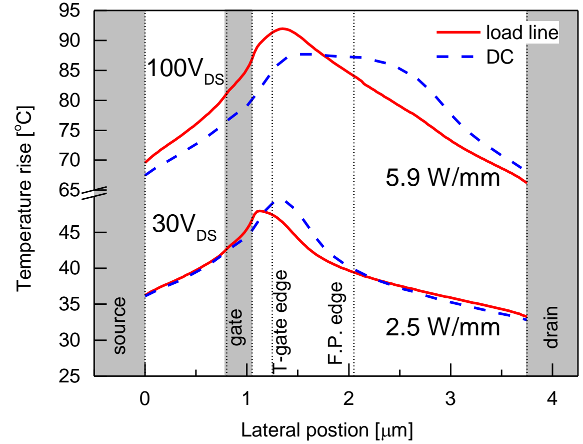

Figure 6: Lateral channel temperature profiles along the AlGaN/GaN interface, simulated using a combined drift diffusion and finite element model. Temperature profiles are plotted for two scenarios: Heating averaged along a class B load line and at a point on the load line with matching power dissipation. Two load lines are considered, at a drain voltage of 30V and 100V.

from this approximation at high frequency, the “ideal” load lines shown in Fig. 3(a) are nevertheless close enough representation for the purpose of modelling the channel self-heating during RF operation.

The gate input voltage varies sinusoidally about a quiescent point during RF operation; for class B operation this is close to the pinch off voltage, as illustrated in Fig. 3(a). By dividing the gate signal into discrete equally spaced time steps, corresponding sample points can be generated on the load lines, illustrated in Fig. 3(a), simply by considering the transistor in series with a resistive load. The transistor channel Joule heating profile is then simulated at each of these points in the IV plane. We note that the sample points are more concentrated when close to the knee voltage in Fig. 3(a). Half of the sample points do not contribute to the heating because the transistor is pinched off and there is no current. The power dissipation “seen” by the transistor channel can be averaged over all of the sample points on the load line since the period of one operating cycle is much less than the device thermal time constant at RF frequencies. Therefore, we average the RF channel heating profile simulated at each of the sample points shown in Fig. 3(a) and use the resulting Joule heating map as an input for the FE thermal model. It is implicitly assumed that the instantaneous current and electric field distribution during RF operation is equal to the corresponding DC (static approximation).

Figure 3(c) shows the modeled channel Joule power dissipation in the transistor channel as a function of drain voltage for the load line sample points shown in Fig. 3(a). The largest self-heating contribution is at the center of the load line, e.g., around $15V_{DS}$ for the 30V load line. The average power dissipation is obtained by integrating over one operating cycle, e.g. for the 30V load line shown, the average P_{diss} is 2.5 W/mm, whereas P_{diss} = 5.9 W/mm for the 100V load line. For comparison, DC bias points matching the average load line power dissipation are shown in Fig. 3(a); these bias points are

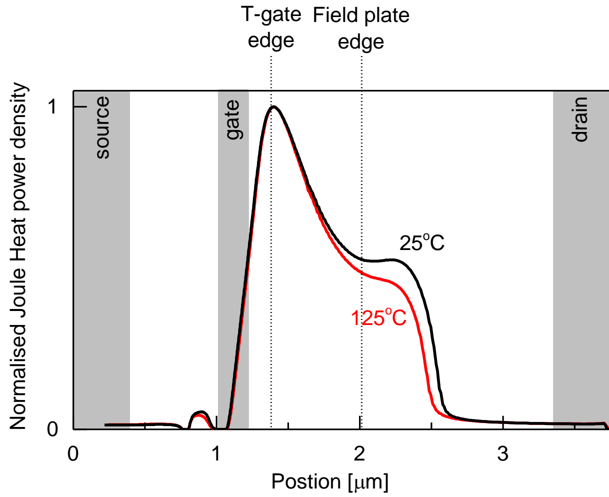

Figure 7: Nomalized simulated Joule heat power distributions in the HEMT channel, 2 nm below the AlGaN/GaN interface, evaluated at two ambient temperatures: 25°C and 125°C. The bias point is $46V_{DS}$ and $-1.42V_{GS}$, corresponding to the centre of the 100V load line.

representative of the DC-HTOL test condition for their respective load lines. These are ideal power dissipation values, only including Joule heating in the transistor channel. Other factors affecting PAE, such as RF losses could be included, although these are second order effects with respect to intrinsic Joule self heating.

IV. Results and Discussion

Raman thermography measurements were performed at a drain current of 100 mA/mm and around $-3V_{GS}$, up to a maximum drain voltage of 100V, a representative bias condition for DC HTOL tests. Figure 4 shows the measured temperatures overlaid with the 3D FE model results, illustrating that the thermal model accurately reproduces the measured average temperature in the GaN channel, in the region illustrated in Fig. 1. The die thermal resistance is also accurately reproduced in the thermal model. The agreement between measured and simulated temperatures enables peak channel temperatures to be predicted with confidence, which are also overlaid in Fig. 4 for comparison. We observe that the measured temperature underestimates the peak channel temperature by 22% at the maximum power dissipation for the 8 finger device investigated here, highlighting the importance using a combination of measured temperatures and simulation to estimate the channel temperature.

The power distribution profile across the channel changes as the drain voltage is increased. Figure 5 illustrates the simulated Joule heat power distribution corresponding to measurement points shown in Fig. 4: At $30V_{DS}$ heating is concentrated under the drain edge of the T-gate overhang, and can be approximated as a ~0.5 µm-long heater at the gate edge. When the drain voltage is increased to 100 V, which is above the field plate threshold voltage, heating extends beyond the field plate edge. Joule heat spreading occurs for two reasons: The electric field spreading effect of the field plate and the punch through effect which distributes current away from the gate edge. The dependence of the channel power dissipation profiles on bias voltage is clearly illustrated in the lateral channel profiles shown in Fig. 5, above ~$50V_{DS}$ a significant proportion of heating can extend beyond the field plate edge. Figure 5 highlights the importance of considering the self-heating bias dependence when modelling channel temperature, particularly at higher drain voltages.

Figure 6 shows a comparison of simulated channel temperature profiles for two cases at matching power dissipation: Averaged Joule heating along the load line and Joule heating at a fixed DC bias point, which is indicated in Fig 3(a). At a drain voltage of 30 V, we observe that the load line average and DC temperature profiles are very similar. There is a small shift of the temperature peak location away from the gate in the DC case, although the difference between the peak channel and peak gate temperatures is negligible, about 1°C. This is consistent with the Joule heating profile shown in Fig. 5, i.e., field spreading is negligible at $30V_{SD}$. In contrast, a significant difference is apparent for the temperature profiles modeled for the 100 V_{DS} case. This is anticipated, since the drain voltage is above the field plate threshold voltage, >60V. Therefore, more spreading of the Joule heating is occurring in the DC case with respect to the load line average, where the majority of the heating contribution is around the center of the load line ($50V_{DS}$).

The spreading of Joule heating at high drain voltage lowers the peak channel and peak gate temperatures with respect to the load line average: The peak gate temperature rise is reduced from 88°C to 80°C (9%). Although this is an extreme example, it does illustrate that at higher voltages there can be a differences in channel temperature when device are operated in RF or DC, even at identical power dissipations. Another important consideration is which temperature is most relevant when evaluating the activation energy of a thermally driven degradation mechanism. We observe a more significant difference between the peak gate (lower) and peak channel (higher) temperature at higher drain voltages. Since device wearout during HTOL tests is often attributed to degradation of the gate, peak gate temperature may be the more relevant parameter when testing at higher drain voltages.

Since the channel temperature in the resulting 3D FE model can differ from that of the 2D drift diffusion model, it is important to consider what effect temperature has on the simulated Joule heating distribution in the HEMT channel. To evaluate this, drift diffusion simulations were run at two ambient temperatures: At 25°C matching the measured chuck temperature and at an elevated temperature of 125°C, as shown in Fig. 7. Comparing the normalized Joule heating profiles in the channel, we observe only a marginal difference in the channel self heating distribution, even when increasing the simulation temperature by 100 °C. This illustrates that the effect of electrothermal interaction on the shape of the Joule heating profile is weak and can be neglected. Another consideration is the electrothermal interaction along the gate finger width, which would redistribute current from the hotter central regions of the HEMT to the cooler outer regions. Although this is not accounted for in the current model, we

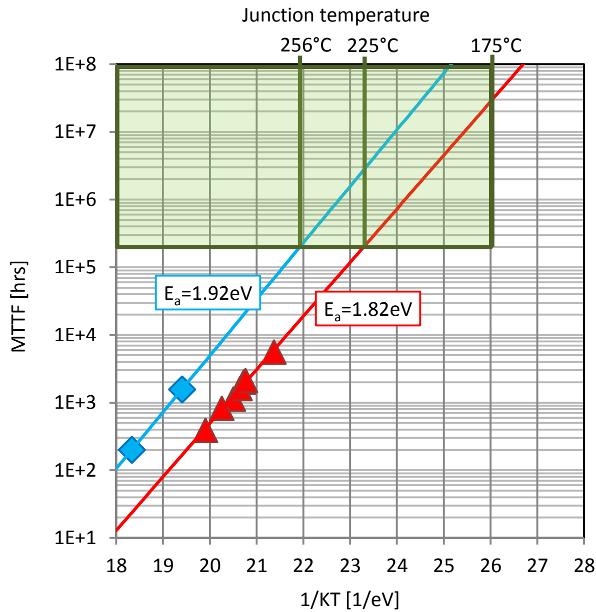

Figure 8: DC HTOL test data obtained at a drain voltage of 50V and 50 mA, and junction temperatures from 270 °C to 310 °C (red triangle symbols, 5-10 DUT per point), adapted from [1]. RF HTOL results (blue diamond symbols, 4 DUT per point) are plotted for comparison. Extrapolations and activation energies obtained using the Arrhenius equation are shown. Junction temperatures were determined from a FE thermal model validated using Raman thermography thermal measurements. The RF junction temperature is assumed to be equal to the DC junction temperature at the equivalent channel power dissipation.

estimate that this effect would reduce the peak temperature rise by less than 2% considering the modelled 22 °C variation in peak channel temperature along the width of the central gate finger in the 100V load line simulation.

Based on the results presented here, we do not expect a significant difference in channel temperature during DC-HTOL and RF HTOL testing when operating GaN HEMTs at typical drain voltages, e.g., below 50V. Therefore, activation energies and MTTFs determined from DC and RF testing are expected to be equivalent, assuming that thermally activated degradation is the dominant wear out mechanism. This is consistent with reports showing that the effects of high temperature DC and RF stress are not substantially different [10, 11]. The results of DC and RF HTOL testing performed at UMS for the GH50-10 technology is shown in Figure 8. An activation energy of 1.82 eV was determined from the DC test results, with an MTTF $>10^7$ hours at an operating channel temperature of 175°C – illustrating the robustness of the GaN technology. For comparison, RF HTOL test have been performed for a select number of devices. The activation energy determined from the RF HTOL test is 1.92 eV, which is very similar to the DC value. Indeed the wear out mechanism in each case is attributed to an increase in gate current and loss of drain current control. However, there is an apparent offset between the RF and DC Arrhenius slopes, with the projected RF lifetime exceeding that of DC: The projected junction temperature at an MTTF of 2×10^5 hours are 256°C and 225°C based on the RF and DC results. This is counter to the modelling prediction that the junction temperature is equivalent during DC and RF operation, or if different at all, marginally lower for DC. Therefore we do not attribute the difference between the DC and RF HTOL results to thermal effects. A possible explanation for the discrepancy observed between the DC and RF HTOL results is that the failure criteria is often different for RF and DC tests. For example, the DC data shown in Fig. 8 is based on a gate current failure criteria, whereas the RF test was run until catastrophic failure, possibly accounting for the time offset observed.

V. Conclusion

RF and DC Joule self-heating in GaN HEMTs operated at the same channel power dissipation has been investigated. Based on the results of an experimentally calibrated combined electrical and thermal model, we predict similar channel temperatures at typical drain voltages, e.g. <50V. Whereas a 9% higher temperature rise is predicted for RF operation at a drain voltage of 100 V, with respect to DC operation. Differences observed when comparing RF-HTOL and DC-HTOL results are therefore unlikely to be attributable to thermal effects, unless high voltage operation is considered.

Acknowledgement

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