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# ENTRA: Whole-Systems Energy Transparency

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## Abstract

Promoting energy efficiency to a first class system design goal is an important research challenge. Although more energy-efficient hardware can be designed, it is software that controls the hardware; for a given system the potential for energy savings is likely to be much greater at the higher levels of abstraction in the system stack. Thus the greatest savings are expected from energy-aware software development, which is the vision of the EU ENTRA project. This article presents the concept of *energy transparency* as a foundation for energy-aware software development. We show how energy modelling of hardware is combined with static analysis to allow the programmer to understand the energy consumption of a program without executing it, thus enabling exploration of the design space taking energy into consideration. The paper concludes by summarising the current and future challenges identified in the ENTRA project.

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## 1. Introduction

Energy efficiency is a major concern in systems engineering. The EU’s Future and Emerging Technologies MINECC programme aims to “lay the foundations for radically new technologies for computation that strive for the theoretical limits in energy consumption.” The research objectives range from physics to software; they include, among others, new elementary devices, as well as “software models and programming methods supporting the strive for the energetic limit.” The ENTRA project, [entraproject.eu](http://entraproject.eu), addresses the latter objective;

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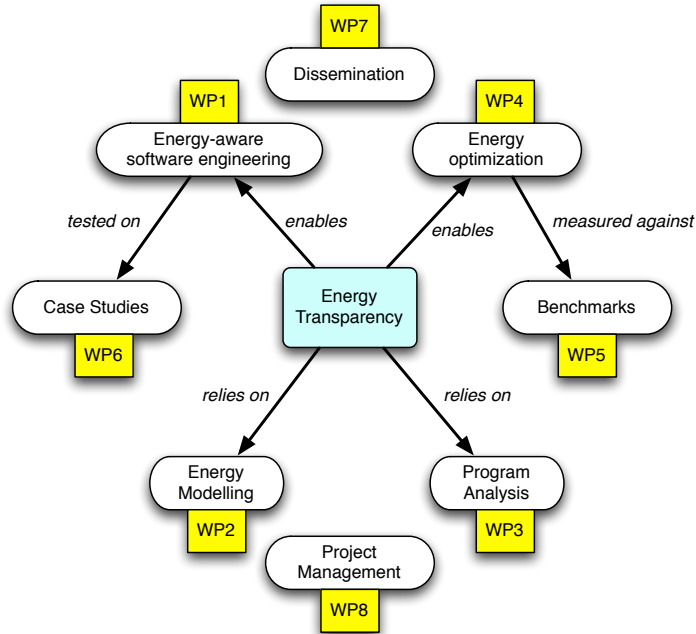


Figure 1: Overview of the ENTRA project work plan

we focus on energy transparency, which we regard as a key prerequisite for new energy-aware system development methods and tools.

The ENTRA project ran from October 2012 to December 2015 (39 months) and was funded by the European Commission under the 7th Framework Programme. The consortium contained three research institutions and one industrial partner specialising in the design of advanced multicore microcontrollers (XMOX xCORE). The overview of the project structure is shown in Figure 1. The foundations for the central concept of energy transparency were developed in two work packages (WP2 and WP3) on energy modelling and energy analysis respectively. Energy transparency enables energy optimisations, studied in WP4. WP1 concerned the development of tools and techniques applicable in energy-aware software development. Finally there were work packages dealing with benchmarking, evaluation, dissemination and project management. This paper summarises mainly the outcomes of work packages WP1, WP2, WP3, WP4 and WP6. The public deliverables of the project are all available on the project website <http://entraproject.eu>.

After this introduction, we discuss the two main areas of research supporting energy transparency. Section 2 presents approaches for building models of software energy consumption at different levels of abstraction. Section 3 contains an overview of static resource analysis techniques, showing how an energy model

can be used in analysis of a program’s energy consumption. Section 4 summarises the role of energy transparency in energy-aware software development, discusses the achievements in the project so far, and outlines current challenges and directions for future research.

### *1.1. Energy-Aware Computing*

Energy-aware computing is a research challenge that requires investigating the entire system stack from application software and algorithms, via programming languages, compilers, instruction sets and micro architectures, to the design and manufacture of the hardware. This is because energy is consumed by the hardware performing computations, but the control over the computation ultimately lies within the applications running on the hardware. While hardware can be designed to save a modest amount of energy, the potential for savings is far greater at the higher levels of abstraction in the system stack. An estimate from Intel [1] is that energy-efficient software can realize savings of a factor of three to five beyond what can be achieved through energy efficient hardware. Roy and Johnson [2] list five objectives that “help make software design decisions consistent with the objectives of power minimization”: match the algorithm to the hardware; minimize memory size and expensive memory accesses; optimise the performance, making maximum use of available parallelism; take advantage of hardware support for power management; and select instructions, sequence them, and order operations in a way that minimizes switching in the CPU and datapath. To achieve these objectives requires the programmer and/or the tools to understand the relationship between code and energy usage. Energy Transparency aims to enable exactly this.

### *1.2. Energy Transparency*

The concept of energy transparency is at odds with the trend in modern software engineering - the desire to abstract away machine-level details using high-level languages, abstract data types and classes, libraries and layers of interpretation or compilation, in the interests of portability, programmer productivity, understandability and software reuse. By contrast, energy transparency requires making visible how software impacts on energy consumption when executed on hardware. Availability of this information enables system designers to find the optimal trade-off between performance, accuracy, and energy usage of a computation. To achieve energy transparency, models of how energy is consumed during a computation are required. As will be discussed in Section 2, such models can be established at different levels of abstraction, ranging from models that characterize individual functional hardware blocks [3], via Instruction Set Architecture (ISA) characterization models [4, 5, 6], to models based on intermediate representations used by the compiler [7, 8]. The final energy models provide information that feeds into static resource usage analysis algorithms [9, 10, 11, 12, 13, 14, 15, 16], where they represent the energy usage of elementary parts of the computation. This is discussed in Section 3.

## 2. Energy Modelling

Energy models can rely on information at several possible abstraction levels, from gate-level hardware description, through functional block and Instruction Set Architecture (ISA), up to performance counter or transaction based abstractions. Energy models at higher levels tend to be faster to use, but have lower accuracy than models at lower levels of abstraction. In ENTRA, the aim was to provide accurate modelling that can be exploited through analysis that is applied in order to estimate the energy consumed by software.

### 2.1. Defining and constructing an energy model

The ISA is a practical level of abstraction for energy modelling, because it expresses underlying hardware operations and their relationship with the intent of the software. Constructing a model at this level gives us the following benefits: energy costs can be attributed directly to individual machine instructions as output by the back end of the compiler; instruction properties and energy consumption are strongly correlated, e.g. energy consumption typically increases with increasing numbers of operands; and machine instructions can be traced back to the original source code statements written by the software developer, as well as to various intermediate representations.

However, energy modelling at the ISA level requires additional effort in order to produce useful models: instruction costs must be captured through a profiling suite and measurement of device power; in addition, indirect or statistical approaches are required to characterise instructions that cannot be profiled through direct measurements. Furthermore, for multi-threaded architectures other properties such as the cost of running multiple threads and the cost of idle periods must be determined.

Our target architecture for energy modelling and analysis is the XMOS xCORE embedded microcontroller [17]. Beyond offering timing-deterministic instruction execution, the xCORE is hardware multi-threaded and comes in a variety of multi-core configurations. The xCORE architecture is simple by design and, thus, ideal to investigate the advanced energy modelling and static analysis techniques required to achieve energy transparency. The techniques we developed are readily transferable to other deeply embedded, cache-less, IoT-type processors such as those in the ARM Cortex M series or the Atmel AVR. The fact that the xCORE offers multi-threading made it a particularly interesting target for the ENTRA project.

We have shown that in the xCORE the number of active threads has an impact upon energy consumption [6]. As such, the model must take this into account. Traditional ISA-level models, such as that of [18], can attribute energy costs simply to instructions, the transitions between instructions, and any additional effects that impact on energy consumption, such as cache hits and misses. Although we build on this principle, parallelism has to be considered, yielding

a more complex model equation for  $E_p$ , the energy consumed by a program  $p$ :

$$E_p = P_b N_{\text{idl}} T_{\text{clk}} + \sum_{t=1}^{N_t} \sum_{i \in \text{ISA}} ((M_t P_i O + P_b) N_{i,t} T_{\text{clk}}) \quad (1)$$

In Eq. (1) the energy consumption is split into two parts, capturing idle and active processor behaviour, respectively. For the former, we consider the *base processor idle power*,  $P_b$ , that is present even when the device is waiting on external events, multiplied by the the number of cycles with no active threads,  $N_{\text{idl}}$ , and the clock period,  $T_{\text{clk}}$ . For the latter, individual instruction costs are accounted for based on their costs  $P_i$ , as well as an aggregated inter-instruction overhead,  $O$ , and a parallelism scaling factor,  $M_t$ , determined by the number of active threads  $t$ . This is calculated for each ISA instruction  $i$ , and multiplied by the number of occurrences in the target program at that particular level of parallelism,  $N_{i,t}$ , as well as the clock period,  $T_{\text{clk}}$ .

Model parameters are separated into two groups. Values for the first group of constants are obtained by profiling the processor for a fixed clock period  $T_{\text{clk}}$ , yielding the base power  $P_b$ , inter-instruction overheads  $O$ , per-instruction costs  $P_i$  and parallelism scaling  $M_t$ ; all measured in  $mW$ . The second group must be determined through analysis of the target program. These include the number of idle cycles,  $N_{\text{idl}}$ , the number of threads,  $N_t$ , in the program, and the instruction counts,  $N_{i,t}$ , for each instruction  $i$  and number of active threads  $t$ . If the analysis can produce these values, Eq. (1) can be used to estimate program energy. We have demonstrated various simulation- and static analysis-based methods that follow this principle.

To illustrate instruction profiling, an example *heat map* representing the device power from interleaving a selected subset of data manipulation instructions is shown in Fig. 2. The profiling framework executes tightly coupled threads through the xCORE pipeline, with random, valid operand values to produce an average power estimate for each instruction. Random input data is shown to cause higher power dissipation than more constrained data that would be found in real-world programs [19], e.g. due to data dependencies, thus creating a modest over-estimate in most cases.

Instruction profiling can only be used to determine the costs of instructions that can be executed repeatedly and in succession. The cost of other instructions can be estimated with a generic average or grouped by operand count [6], or more accurately through a regression tree approach that identifies the most significant of a set of features, including instruction length, whether memory is accessed and others, to find the most similar directly profiled instruction [20]. The latter is the most accurate of the three approaches and adds no significant modelling overhead.

This form of model can be used by various analysis methods. An Instruction Set Simulation (ISS) can produce an instruction trace from which the instruction counts and thread activity can be determined. A cycle-accurate ISS will achieve the best model accuracy. Alternatively, per-thread instruction execution statistics can be used instead to extrapolate the model terms. This is faster



than producing a full trace, but can increase estimation error. It has been shown to yield an acceptable  $\pm 10\%$  margin in benchmarks [6].

As we will see in Section 3, the program-dependent terms in the model can be calculated by static analysis, removing the simulation step and allowing rapid design-space exploration, as well as parameterised, bounded energy estimations. The values of  $N_{i,t}$  and  $N_{\text{idl}}$  can be analysed as functions of the input state. This allows the derivation of energy functions characterising the energy consumption of all possible runs of a program, rather than a specific run or set of runs.

In our experiments, tracing was up to two orders of magnitude slower than statistics-only simulation, the latter typically taking less than one minute. However, this can be mitigated by analysing single functions or blocks, ignoring other parts of the trace, and terminating as soon as the blocks of interest have been executed, making trace simulations take less than a minute in most of the cases we observed. Static analysis can, of course, achieve faster results, by analysing the same code blocks without simulation.

A key prerequisite for achieving high accuracy in energy modelling at the ISA level is a predictable, time-deterministic architecture, where the instruction set gives an accurate view of how the processor will behave. The xCORE’s thread scheduling and cache-less SRAM memory subsystem, together with the absence of performance enhancing complexity in the micro-architecture, enabled us to achieve a very accurate model, which is essential to obtaining accurate energy predictions. Thus, as for worst case execution time (WCET) analysis, the results of energy modelling and energy consumption analysis are influenced by processor architecture, and predictability determines the accuracy achievable as well as the complexity of the modelling and analysis techniques [21].

## *2.2. Multi-core energy modelling*

For a multi-core system the ISS must accurately simulate the network behaviour in order to capture the timing and link-traversal of data. This allows accurate estimation of communicating multi-core processes [20]. Static analysis must provide similar characterisation, therefore instruction execution, network behaviour and the flow of communication between processes, must be predictable in order to enable energy transparency. The single-core, multi-threaded processor model achieves an average error of 2.7% over a suite of single- and multi-threaded benchmarks, with a standard deviation of 4.4%. The multi-core model demonstrates an average energy estimation error of  $-4.9\%$  with a standard deviation of 3.9%. Models with less than 10% error provide suitable accuracy for energy estimations.

## *2.3. Energy modelling at higher levels of software abstraction*

Performing static analysis at the ISA level can benefit from good accuracy due to its closeness to the hardware, but it can suffer from a loss of useful information such as program structure and types [22]. A good compromise is found by modelling at the Intermediate Representation (IR) used by compilers, where program information is preserved. Since the compiler is the natural place



for optimisations, modelling and predicting the energy consumption at IR level could therefore enable energy specific optimisations.

Using a mapping technique, we lifted the energy model in Eq. (1) to the IR level of the compiler [8], implemented within the LLVM tool chain [23]. ISA level energy models can thus be propagated up to LLVM IR level, allowing energy consumption estimation of programs at that level. This enables static analysis to be performed at a higher level than ISA, thus making energy consumption information accessible directly to the compiler and optimiser.

The mapping technique determines the energy characteristics of LLVM IR instructions. It provides on-the-fly energy characterization that takes into consideration the compiler behavior, control flow graph (CFG) structure, types and other aspects of instructions. Taking into account such information improved the accuracy of the LLVM IR characterization significantly. The experimental evaluation demonstrated that the mapping technique allowed for energy consumption transparency at the LLVM IR level, with accuracy keeping within 1% of ISA-level estimations in most cases [8].

In principle, the same mapping technique may be used to map the energy consumption of programs to even higher levels, such as the source code. However, a fine grained characterization for each line of source code using this method is impractical due to the numerous transformations and optimisations introduced by the compiler and the loss of accuracy resulting from the difficulty of associating energy consumption costs obtained at lower levels to source code lines.

An alternative approach to building a source-level energy model was investigated in [24]. The target language here was Java on the Android platform; any attempt to map a lower-level energy model up to the source code would need to deal explicitly with the Java virtual machine as well as operating system layers, a highly impractical strategy. Instead, the basic energy-consuming operations from the source code are identified and the correlations to energy costs are found by measuring energy consumption in a large number of execution cases and analyzing the results using techniques based on regression analysis. The resulting energy model of the basic operations implicitly includes the effect of all the layers of the software stack down to the hardware. The approach is inherently approximate; nevertheless such an approach may be the only feasible one in complex software stacks, when source-level energy models are needed, for instance to give the source-code programmer an energy profile of the code under development.

### 3. Static Analysis of Energy Consumption

Static analysis is the other key component of energy transparency. It infers information about energy consumed by programs without actually running them. As with energy models, analysis can be performed on program representations at different levels in the software stack, ranging from source code (in different programming languages) to intermediate compiler representations (such as LLVM IR [23]) or ISA.

Static analysis at a given level consists of reasoning about the execution traces of a program at that level, in order to infer information (among other things) about how many times certain basic elements of the program will be executed. The role of the energy model is to provide information about the energy consumption of such basic elements; it is used by the analysis to infer information about energy consumption of higher-level entities such as procedures, functions, loops, blocks and the whole program.

Analysis can also be performed at a given software level using energy models for a lower level. Such a model needs to be mapped upwards to the higher level, as described in Section 2.3. The information inferred by static analysis at a lower level can also be reflected upwards to a higher level using suitable mapping information.

In the ENTRA project, this approach has been applied to the static analysis of XC programs running on xCORE architectures. However, our framework is language- and architecture-neutral. We will return to this in Section 4.

### *3.1. Analysis/modelling trade-off*

Our hypothesis was that the choice of level affects the accuracy of the energy models and the precision of the analysis in opposite ways: energy models at lower levels will be more precise than at higher levels while at lower levels more program structure and data structure information is lost, which often implies a corresponding loss of accuracy in the analysis. This hypothesis about the analysis/modelling level trade-off (and potential choices) is illustrated in Figure 3.

In ENTRA we have explored different points in this space of combinations of analysis and modelling. Our experimental results [25] confirm that the expected trade-off exists, but also suggest that performing the static analysis at the LLVM IR level is a good compromise. LLVM IR is close enough to the source code level to preserve most of the program information needed by the static analysis, whilst close enough to the ISA level to allow the propagation of the ISA energy model up to the LLVM IR level without significant loss of accuracy.

### *3.2. Information inferred by analysis*

The information inferred by the analyzers is guided by its final use: program optimisation, verification, helping energy-aware software developers to make design decisions, and so on. For example, they can infer safe approximations, namely upper and lower bounds, on the energy consumed by the program or parts of it. These approximations can be functions parametrised by the sizes of the input data and other hardware features such as clock frequency and voltage. The analyzers can then infer concrete values of the parameters that yield the worst-case energy consumption of the program or its parts.

Static energy profiling [26] determines the distribution of energy usage over the parts of the code. This can be very useful to the developer, showing which parts of the program are the most energy-critical. Some functions or blocks in the program are perhaps not particularly expensive in energy in themselves but

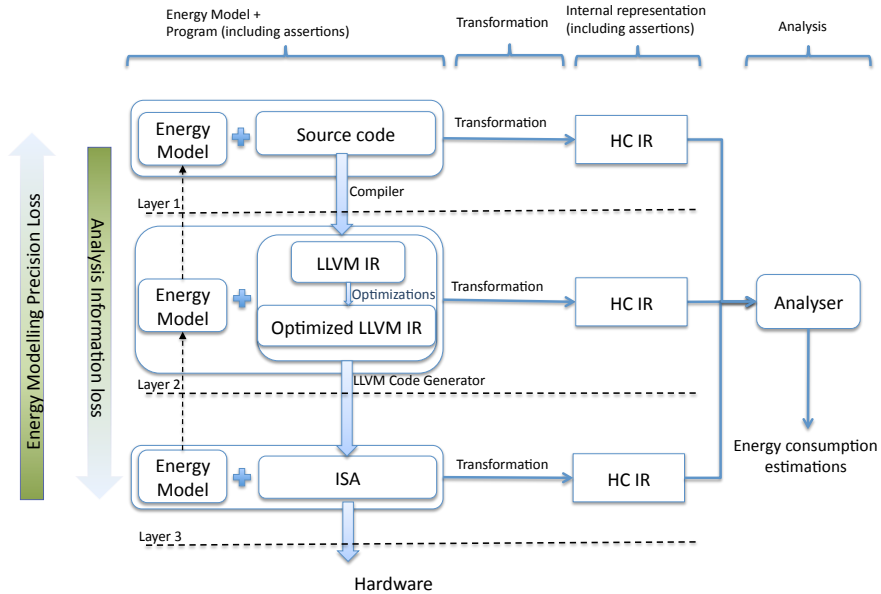


Figure 3: Analysis/modelling level trade-off and potential choices [25]

are called many times. Such parts are natural targets for optimisation, since there a small improvement can yield considerable savings.

Note that the safety of bounds depends on energy models giving safe bounds for each instruction. This is a challenging problem which is discussed in Section 4. Safe bounds are vital for applying energy analysis to verifying or certifying energy consumption.

### 3.3. A generic resource analysis framework

The resource analysis framework that we have developed is parametric with respect to *resources* and *programming languages*. Regarding resources, the common assertion language allows the definition of different resources and how basic components of a program affect the use of such resources. More concretely, it allows the encoding of different energy models for specific hardware architectures, and, in particular, the energy models developed for the xCORE architecture at the LLVM IR and ISA levels, described in Section 2.

Regarding programming languages, we differentiate between the *input language* (which in ENTRA can currently be XC source, LLVM IR, or ISA) and the *intermediate semantic program representation*, which is what the resource analysis actually operates on. We use *Horn Clauses* as the intermediate program representation, referred to as the “HC IR.” A transformation is performed from each supported *input language* into HC IR, which is then passed to the

resource analysis. We have explored different approaches for this transformation. One approach is to perform a *direct* transformation into HC IR, and this has been applied both to ISA and LLVM IR code [22, 25]. Another approach consists in producing the HC IR by applying partial evaluation techniques to instrumented interpreters that directly implement the semantics of the language to be analysed [27]. In both cases, the resulting HC IR programs are analysed by the CiaoPP tool (see Section 3.5).

Horn Clauses offer several features that make them convenient for analysis [28]. For instance, this representation inherently supports Static Single Assignment (SSA) and recursive forms. There is a current trend favouring the use of Horn Clause programs as intermediate representations in analysis and verification tools [29, 30, 31, 32].

Using the generic HC IR representation, the assertion language and the CiaoPP analysis tools, we have instantiated the general framework to produce a series of concrete energy analyzers which have allowed us to study the advantages and limitations of different techniques as well as the trade-offs implied by different choices of analysis and energy modelling levels.

#### 3.4. A common assertion language

We have defined a common assertion language as a vehicle for propagating energy-related information throughout the system levels, and for communication among the different analysis, verification, and optimisation tools, and the actors involved in software development. This assertion language allows expressing energy models for different architectures, writing energy consumption specifications, describing energy consumption of components that are not available at analysis time, expressing analysis results, and ensuring interoperability. We refer the reader to [33] and its references for a full description of the Ciao assertion language that is the basis for the assertions used in the HC IR, and the (internal) common assertion language of ENTRA [34]. The ENTRA common assertion language also includes a front end to express energy specifications and other energy related information in the XC source code.

#### 3.5. Energy analysis using CiaoPP

The input to the CiaoPP parametric static resource usage analyzer [13, 14, 15] is the HC IR, along with assertions in the common assertion language expressing the energy model for LLVM IR blocks and/or individual ISA instructions, and possibly some additional (trusted) information. The analyzer is based on an approach in which recursive equations (cost relations), representing the cost of running the program, are extracted from the program and solved, obtaining upper- and lower-bound cost functions (which may be polynomial, exponential or logarithmic) in terms of the program’s inputs [9, 10, 11, 12, 16].

These output cost functions express the energy consumption for each block in the HC IR, which can be mapped directly back to the language represented by the HC IR.

The generic resource analysis engine is fully based on *abstract interpretation* [15], and defines the resource analysis itself as an *abstract domain* that

is integrated into the PLAI abstract interpretation framework [35] of CiaoPP. This brings in features such as *multivariance*, efficient fixpoints, and assertion-based verification and user interaction. The setting up and solving of recurrence relations for inferring closed-form functions representing bounds on the sizes of output arguments and the resource usage of the predicates in the program are integrated into the PLAI framework as an abstract operation.

### 3.6. Direct energy analysis of LLVM IR

As mentioned, LLVM IR offers a good trade-off between analyzability and accuracy. In addition to using a generic approach based on CiaoPP and a translation to HC IR, the ENTRA project has experimented with an approach that uses similar analysis techniques but operates directly on the LLVM IR representation [36]. The advantage is that this approach can be integrated more directly in the LLVM toolchain; in principle it is applicable to any languages targeting LLVM. The energy model used is exactly the same as the one applied in [25] and described in Section 2.1.

### 3.7. WCET-inspired energy consumption static analysis

Since the underlying challenges of analysing the timing and energy consumption behaviour of a program appear to be quite similar, in [8], we have applied well known WCET analysis techniques to retrieve energy consumption estimations. One of the most popular WCET techniques is implicit path enumeration (IPET) [37], which retrieves the worst case control flow path of programs based on a cost model that assigns a timing cost to each CFG basic block. We have replaced the timing cost model by the ISA energy model given in Equation (1). In the absence of architectural performance enhancing features, such as caches, this technique can provide safe upper bounds for timing. Through our experimental evaluation we have demonstrated that this is not the case for energy, as energy consumption, in contrast to time, is data sensitive (see Section 4).

In order to explore the value and limits of applying IPET for energy consumption estimations, we have also extended the analysis to the LLVM IR level, using the LLVM IR energy characterization given by the mapping technique referred to in Section 2.3. Furthermore, we have extended the energy consumption analysis to multi-threaded embedded programs from two commonly used concurrency patterns: task farms and pipelines. The experimental evaluation on a set of mainly industrial programs demonstrates that, although the energy bounds retrieved cannot be considered safe, they can still provide valuable information for energy aware development, delivering energy transparency to software developers in the absence of widely accessible software energy monitoring.

### 3.8. Probabilistic resource analysis

Bounds on energy consumption are useful, but information about the distribution of consumption within those bounds is even more so. For example, it may be that most execution cases of a program result in consumption close to the lower bound, while the upper bound is reached only in a few outlying

cases, or vice versa. From the distribution, estimates of average energy consumption can be derived. One approach to obtaining this kind of information is to perform probabilistic static analysis of a program with respect to its energy consumption. This is a special case of probabilistic output analysis, whose aim is to derive a probability distribution of possible output values for a program from a probability distribution of its input. The output in this case is energy consumption [38, 39].

#### 4. Discussion

Energy-aware software development needs energy transparency; designers and programmers have to understand energy consumption at an early stage in the development lifecycle in order to explore the design space taking energy consumption into consideration. Many decisions taken early in the process, such as the hardware platform, the degree of parallelism, fundamental algorithms and data structures, can determine the overall energy efficiency of the final application. The energy-aware software development lifecycle includes activities such as:

- Providing an energy specification or energy budget.
- Making initial rough estimates of energy consumption based on high-level models of the application, allowing exploration of design space with respect to energy consumption.
- Choosing and configuring a hardware platform which suits the application, for example reducing the energy cost of frequent communications or memory accesses.
- Developing code with constant reference to the energy consumption of program parts, allowing energy “bugs” to be identified early.
- Performing energy optimisation of critical code sections using more precise energy models and taking into account the compiler generated machine instructions.
- For energy critical applications, providing guarantees in the form of tight upper and lower bounds on energy consumption.

It is important to note that the development platform is seldom the same as the final deployment platform, emphasising the importance of energy modelling of the final target hardware. The alternative to energy transparency is to wait until the application is run on the final intended platform and then measure its energy usage. At this stage it is likely to be too late to do much about excessive energy consumption.

#### 4.1. Software energy modelling challenges

Verification of worst-case energy consumption requires the development of a worst-case energy model. This is difficult, since the energy cost of executing an instruction depends on the operands. To obtain the worst-case consumption for an instruction we must therefore measure its execution with the operands that induce it. The energy models built in ENTRA are based on averages obtained from measuring the energy consumed when random, valid data is being processed. We demonstrated that the variation due to data can range from 5 to 25% [8]. In [19] we examine the impact of operand values on instruction level energy consumption and propose a probabilistic approach to developing worst-case energy models suitable for safe worst-case energy consumption analysis.

Data-sensitive energy modelling is a serious challenge. Determining the maximum amount of circuit switching between instruction data tends to take an exponential amount of time to evaluate, making it difficult to determine or guarantee the worst case data for an instruction sequence [40]. Even if a model is built where the energy consumed by an instruction is given as a function of its operands, there would still be further challenges in encoding these functions in a suitable way to be exploited effectively by static analysis algorithms.

In [41] we have explored a technique that models both, upper and lower bounds on the energy of “branchless” blocks of instructions, in order to take into account the inter-instruction switching costs within a block. It uses an Evolutionary Algorithm for a faster exploration of the search space, which is also reduced by the fact that the algorithm does not have to deal with the control-flow of the program. Then, such block-level model is fed into a static analysis, which takes into account the program control-flow, and infers energy information for the whole program and its procedures.

#### 4.2. Software energy analysis challenges

Static analysis always involves a trade-off of precision against complexity of the analysis. Obtaining tight bounds of energy usage depends on several factors, including accurate propagation of data size measures and extraction and solution of the relations expressing energy consumption in terms of data sizes. Both of these problems are solvable for a large class of useful programs, but if program structure departs from standard patterns, precision may be rapidly lost. For instance, our realisation of the general framework described in Section 3.3 using the CiaoPP resource analyser described in Section 3.5 (which uses the HC IR) can deal with recursive programs, including multiple and mutual recursion (e.g., divide-and-conquer programs), iterative programs with nested loops, numeric/arithmetic programs, or programs operation on complex data structures such as nested lists and arrays. The analysis produces parametrised energy bounds (which depend on input data sizes) expressed by a large class of functions (e.g., polynomial, factorial, exponential, logarithmic, and summations), in contrast to other approaches that are limited to polynomial functions, or to non-parametric (i.e., absolute) bounds.

The experiments reported in [25] with this realisation of the analysis framework perform the analysis at the ISA and LLVM IR levels, and compare the

energy values obtained by evaluating the inferred energy functions for different input data sizes, with actual hardware measurements (on the xCORE platform). The results show that our LLVM IR level analysis is reasonably accurate (less than 6.4% average deviation vs. hardware measurements) and more powerful than the analysis at the ISA level, in the sense that it can deal with a larger class of programs (e.g., programs involving structured types). The average deviation for the smaller set of benchmarks for which the ISA-level analysis produced non-trivial results was 3.9%. Although we have tested our prototype tools with relatively small programs, they exhibit features that are also present in bigger real programs, and could be analysed at a bigger scale too, since we have designed our analysis tools to enable scalability. Thus, we interpret our experimental results as very promising, and encourage us to continue our research following an incremental approach. Making our prototype tools more robust, powerful and scalable, as well as evaluating them with bigger real programs, is an implementation (and research) challenge in itself.

As already said, our approach to developing energy analysers is architecture neutral, a claim that is supported by the experimental results in [36], performed with the direct energy analysis of LLVM IR described in Section 3.6, for both the ARM Cortex-M and XMOS xCORE platforms. The benchmarks also contain nested loops (some of them with complex control flow predicates) and perform bitwise operations, as well as operations on arrays and matrices. Overall, the final deviation vs. hardware measurements is typically less than 10% and 20% on the XMOS and ARM platforms respectively, showing that the general trend of the static analysis results can be relied upon to give an estimate of the energy consumption. Instantiating our general approach to more platforms (which include the hardware and operating system) and assessing it in different application domains is another challenge that we intend to address in future work.

Static analysis of multi-threaded code is difficult since precision is easily lost due to thread interleaving. Accurate analysis of the timing and synchronisation behaviour of threads is a pre-requisite for energy analysis using the model given in Eq. (1), in which the energy of an instruction depends on how many threads are active simultaneously.

#### *4.3. Extending results to less predictable architectures*

The ENTRA approach is generic and architecture-neutral; that is, it consists of a framework parametrised by an energy model and generic static analysis tools. Front-ends that translate code into a common, analysable form such as HC IR or LLVM IR can in principle be constructed for any programming language. However, much experimentation and investigation remains to be done to apply the approach effectively to architectures that contain sources of unpredictability such as caches, complex pipelines and interrupts that are not present in the xCORE architecture. A likely path of research is to follow the approach in WCET analysis of such unpredictable architectures, employing supporting analyses to permit more accurate energy analyses. An example is approximation of cache contents at specific program points, leading to more accurate models when



it can be guaranteed that a memory access will definitely hit or definitely miss the cache.

#### *4.4. Energy optimisations enabled by energy transparency.*

Different types of optimisations at different levels of the software stack can be performed by taking advantage of the information provided by the multi-level and multi-language ENTRA tools. Both static and dynamic energy optimisations are enabled by energy transparency, which have been investigated in ENTRA. For dynamic optimisations, a framework for energy-aware stochastic scheduling based on evolutionary algorithms (EAs) has been developed, for the cases where tasks are independent [42] and dependent [43]. In the latter case, dependence has been modelled by using copula theory [44], in particular Archimedean copulas [45]. EAs have also been used to improve energy-aware allocation and scheduling for DVFS-enabled multicore environments. For example, the algorithms described in [46, 47] are able to deal with task migration and preemption; and the ones in [48] allow decreasing program accuracy (by performing loop perforation) in order to save energy.

Other optimisations include the use of energy analysis to choose software parameters in order to transform programs to ensure that an energy target is met while minimizing the loss in quality of service. Energy performance has also been improved by optimisation techniques for task placement on an xCORE network after identifying communication patterns among tasks. Using Swallow, an experimental open platform of many xCOREs [49] as a source of model data, it has been demonstrated that incorporating network-level energy consumption and timing into the energy modelling process can aid in identifying the impact of sub-optimal task placement in communicating multi-core applications [50].

Some energy optimisations have already been incorporated into the recently released XC compiler by XMOS Ltd. These optimisations in the object code are obtained by aggressively applying global dataflow analyses inspired by ENTRA project research. Results on case studies, showing a power reduction of approximately 25% by using the global optimiser, can be found in an ENTRA project report [51].

An experiment on energy optimisation of Android code was carried out using the source code energy modelling mentioned in Section 2.3. The energy consumption of battery-driven mobile devices such as smartphones is of increasing concern to developers of software for such devices. The study concerned the optimisation of code for interactive games. The energy model combined with execution profiling, enabled the developer to discover that 10 code blocks (out of several hundred blocks in the considered code) consumed over 50% of the overall energy. Aggressive source code optimisation and refactoring of these blocks enabled energy savings of 6% to 50% in various use-case scenarios [52].

## **5. Conclusions**

The goal of the ENTRA project was to provide techniques and tools supporting energy transparency at the software level. The results obtained include

energy models for the xCORE processor at different levels of abstraction, from ISA level to LLVM IR, as well as preliminary energy models for less predictable architectures. A model incorporating multi-core execution on the xCORE has also been developed. These models are incorporated in static analyses at the corresponding level of code. Experiments have compared predictions of energy consumption for single-threaded programs with actual measured consumption, and encouraging results with only a few percentage of error were obtained. In addition, the trade-offs between accuracy and analysability at different levels were explored, leading to a preliminary conclusion that analysis at LLVM level provides a good compromise. The project identified challenging problems for future research, extending the analyses to multi-threaded code, and building data-sensitive energy models.

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